A Navigation-Grade MEMS Accelerometer based on a Versatile Front End

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***Abstract*—This paper presents a MEMS-based 5th-order ΔΣ capacitive accelerometer. The ΔΣ loop is implemented in mixed signal, the global 5th-order filter having a 2nd-order analog and a 3rd-order digital part. The system can be used with a wide range of sensors, because the mixed-signal front-end is programmable. The developed ASIC comprises a voltage-mode preamplifier, two parallel demodulators implementing CDS, and a 7-bit internally non-linear flash ADC. The latter drives a 3rd-order digital filter which can be configured for different sensor parameters in order to ensure overall loop stability and to optimize the noise performance. With a low-noise MEMS sensor, the system achieves a 19-bit DR and a 16-bit SNR, both over a 300-Hz bandwidth.**

I. INTRODUCTION

The market for inertial high-performance accelerometers can be segmented into several categories: tactical grade, navigation grade and military grade, each characterized by an order-of-magnitude improvement on bias stability, linearity and noise.

Penetrating the inertial-navigation-grade market requires competing from established technologies like macro-electro-mechanical servo accelerometers and quartz-resonating accelerometers. While the macro-electro-mechanical accelerometers reach high performances, they are expensive and fragile [1]. Quartz resonators have excellent dynamic range but exhibit degraded stability performance and very-low-g shock tolerance. MEMS have the potential of low-cost high-volume production thanks to its batch-processing manufacturing. They can also be made very-high-g shock tolerant, without post-shock performance degradation.

Mid- to high-performance open-loop MEMS accelerometers are commercially available today and reach tactical-grade performances with a stability of 1.5mg or 150ppm, a total harmonic distortion of 50dB and an SNR of 97dB [2]. The ultimate evolution of the open loop MEMS sensor is seen at a stability of 10ppm, a THD of 60dB and an SNR of 140dB [1]. Bringing MEMS accelerometer one step further towards higher-performance navigation grade requires operating the MEMS accelerometer in a servo mode. MEMS servo accelerometers have already demonstrated high performance in low-g applications for earthquake monitoring or geoseismic imaging. Noise floors as low as -145dBg/√Hz, with a working range of ±0.3g including 1g gravity compensation have already been reported [3]. The challenge to bring this technology towards inertial navigation is about significantly improving the bias stability. Compared to other previously reported works [4], [5], our design takes advantage of the extremely good mechanical characteristics of the sensor and therefore allows for relaxed requirements on the electronics side. The sensor's mechanical bias stability has been demonstrated to be a key contributor to the overall bias-stability budget even in servo-loop operation.

This paper presents a versatile accelerometer system based on a reconfigurable front-end and a ΔΣ loop. It consists of an application-specific integrated circuit (ASIC) containing a versatile analog front end, a low-precision internally non-linear ADC, and an external digital filter. The versatile electronics can be interfaced with a large variety of sensors for different applications.

Section II presents the system architecture. The different blocks are detailed in section III, while section IV presents measurement results and section V concludes.

II. SYSTEM ARCHITECTURE

Figure 1 presents the architecture of the accelerometer system [6]. The capacitive MEMS accelerometer sensor is a moving mass in the middle between two fixed plates. These three electrodes are connected to a set of high-voltage (HV) switches that apply actuation and position-sensing pulses. An additional HV switch connects the middle electrode to the

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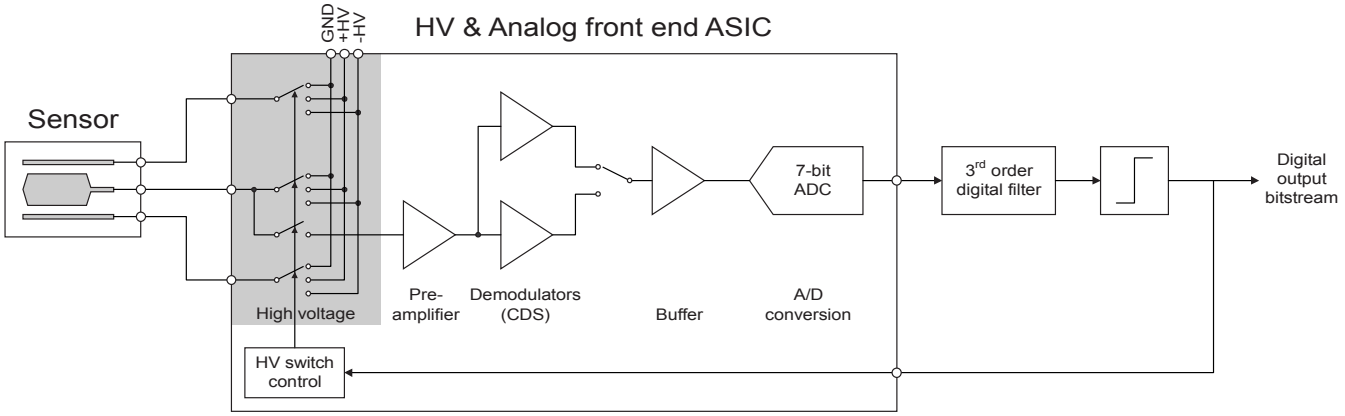

Figure 1. System architecture.

low-voltage (LV) preamplifier in the analog front end during position sensing, and protects the LV circuit during HV actuation of the middle electrode. The analog front-end ASIC is a high-speed low-precision position measurement interface consisting of a low-noise voltage-mode preamplifier, demodulators for correlated double sampling (CDS), and an internally non-linear 7-bit flash analog-to-digital converter (ADC). The gain of each block is configurable to fit the sensor characteristics.

Since the sensor already integrates the input and feedback signals of the ΔΣ loop twice, the precision requirement on the analog front end is relaxed: 7-bit precision gives sufficiently good noise and distortion performance for all the different sensors to be used with the system. The digitized output is fed into a 3rd-order digital filter that increases the loop order to five, giving the system a high resolution. Finally, the sign of the output of the digital filter, which is the output bitstream, also determines the direction in which the actuation force is applied to the sensor.

III. System Blocks

This section presents the different blocks constituting the accelerometer system.

A. Sensor and Front End

The sensor and its interface comprising the HV switches and the preamplifier from Figure 1 are detailed in Figure 2.

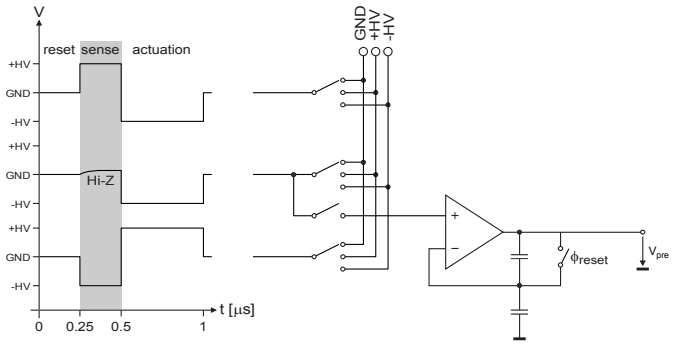

Figure 2. Sensor and analog front end.

The HV-switch control signals are shown for a typical operating cycle. The 1-µs cycle period is subdivided into one position-sensing phase and one actuation phase which are equal in length (0.5µs each). The electrostatic actuation force is generated by connecting the moving mass and one plate to one of the HV supplies, and the second plate to the opposite HV supply.

The position-sensing phase starts by short-circuiting the three sensor electrodes to ground in order to discharge the sensor capacitances (reset). Then the two fixed electrodes are connected to the positive and negative HV supplies, and the moving-mass electrode is connected to the high-impedance input of the preamplifier. Since the sensor capacitance values reflect the position of the moving mass, the middle point of the sensor capacitive bridge displays a corresponding voltage variation. If $C_t(x)$ is the capacitance between the top plate and the middle electrode, $C_b(x)$ between the bottom plate and the middle electrode, and x is the distance of the moving mass to its equilibrium point in the middle between the electrodes, the middle-electrode voltage V_{mid} during the sense phase depicted in Figure 2 is:

$$V_{mid}(x) = -HV + 2HV\frac{C_t(x)}{C_t(x)+C_b(x)} \qquad (1)$$

Since the feedback control loop tries to keep the moving mass in the middle between the top and bottom plates, the displacement of the mass is so small that $C_t(x)$ and $C_b(x)$ vary linearly and symmetrically around a nominal value C_0 with sensitivity C_Δ:

$$C_t(x) = C_0 + C_\Delta \cdot x \quad ; \quad C_b(x) = C_0 - C_\Delta \cdot x \qquad (2)$$

Equation (1) then simplifies to:

$$V_{mid}(x) = HV \cdot \frac{C_\Delta}{C_0} \cdot x \qquad (3)$$

This voltage is amplified by the voltage-mode preamplifier with a capacitive feedback, which is reset prior to amplification. The sign of the output signal can be reversed by exchanging the positive and negative HV supply connections to the top and bottom plates (+sense and −sense in Figure 3), which then allows to perform CDS as discussed in the next section.

The gain of the voltage-mode preamplifier stage is fixed by a capacitor ratio and does not depend on the sensor capacitance value, as it does in charge-mode amplifier topologies [7]. This allows setting the gain of the preamplifier precisely. A low gain value of 10 is chosen to achieve accurate settling within 250ns. A second advantage of the voltage amplifier is that the noise performance is increased [8].

B. Demodulation & CDS

Figure 3 shows one demodulator circuit implementing the CDS, as well as the corresponding switch control signals.

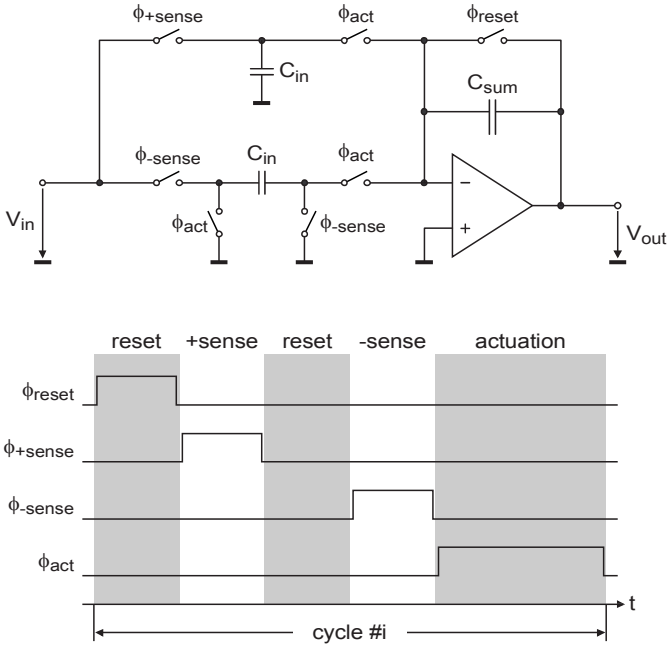

Figure 3. Demodulator and CDS implementation.

The circuit subtracts the pre-amplified signals resulting from two successive +sense and −sense phases during the same cycle, which has the effect of cancelling the offset and 1/f noise of the preamplifier.

The signal is sampled directly on the input capacitors at the end of each sense phase. The charge is then transferred to the summing capacitor during the actuation phase, allowing 500ns for the amplifier to settle and thus relaxing its gain-bandwidth (GBW) design constraints. To accommodate for different sensor characteristics, the gain of the demodulator can be programmed by adjusting the feedback capacitor (C_{sum}).

The disadvantage of the scheme presented in Figure 3 is that because there are two reset and sense phases, the cycle becomes longer. To overcome this limitation, the two sense phases needed for CDS can be part of two successive cycles. There is then only one reset and sense phase per cycle, the +sense and –sense being alternated from cycle to cycle. However, the demodulation output can then be calculated only every second cycle, which reduces the effective ΔΣ loop frequency and decreases performance.

It is also possible to implement the scheme of Figure 4, which uses two demodulators in a time-interleaved fashion. Then each cycle contains either a +sense or a –sense phase. When the first demodulator is performing its first demodulation operation, the second demodulator already finishes the second one and the value computed is fed out. During the next cycle, the roles are reversed and so on. In this way, there is one output value for each cycle without needing two sense phases per cycle or increasing the cycle length. Compared to Figure 3, only one cycle of excess loop delay remains. The optimum choice of the CDS scheme to use depends on the sensor used, the required signal bandwidth, and the required noise performance.

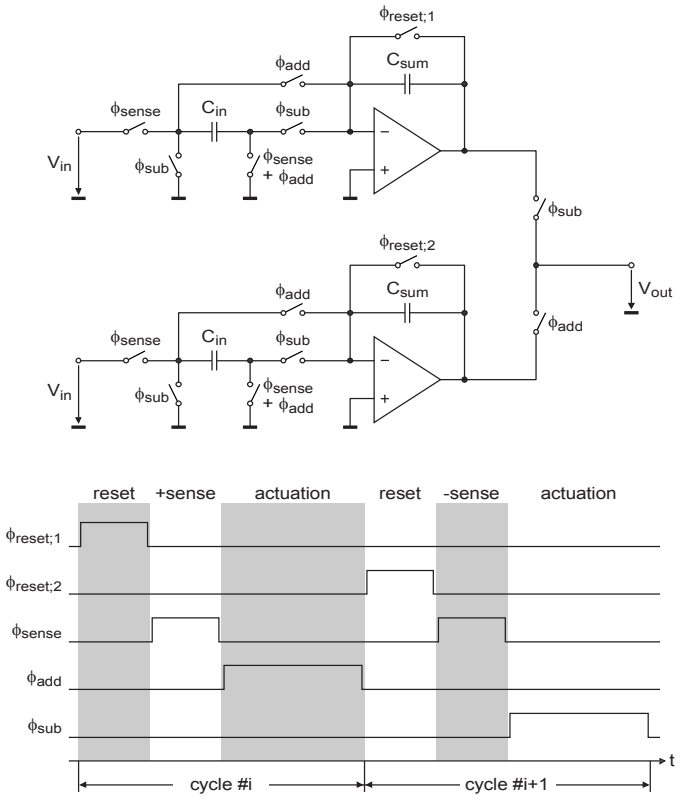

Figure 4. Time-interleaved CDS using 2 demodulators.

C. Analog-to-Digital Conversion

The output of the analog front end is digitized by a low-precision ADC, which is also integrated in the ASIC. The speed and precision requirements are the same as for the analog circuit, i.e. 1MS/s with 7-bit precision. An internally non-linear flash implementation is used [9].

Inside our ΔΣ loop it is not necessary to build a linear 7-bit ADC. The probability distribution at the input of the ADC is not uniform, in most cases there are more values to process in

the centre of the ADC range than towards the extremes. This fact has been used before in multi-bit ΔΣ converters by using complex μ-law ADCs [10] or — easier to implement — semi-uniform quantizers [11]. According to [12], a quantizer can be made optimum if the probability density of its input values is known.

The question is: which probability distribution shall we choose if we do not know much? Simulations and measurements of an acceleration sensor loop have shown that the specific distribution depends on the signal at the input, the sensor, and the parasitic effects like offset and electronic noise. A ΔΣ accelerometer loop — like most other ΔΣ sensor loops too — uses high-gain feedback to keep the sensor mass at a given centre position. The sensor displacement is then small compared to the maximum possible displacement before the sensor mass touches the top or bottom plate. However, since the distributions look so different for different input signals, we have no further knowledge about the probability distribution except that we measure a location parameter with hard bounds far away from the operating range.

Therefore, the distribution to assume is the one which makes no implicit assumptions other than that we measure a location parameter. This is the so-called maximum-entropy distribution for location parameters, which is the Gaussian distribution [13]. So we do not choose the Gaussian distribution because we know that the values to be measured will have that distribution — they often have not — but because it it is the best representation of our prior knowledge: the user of our system can attach different sensors, do different applications, have different input signals, and we do not know what probability distributions to expect, just that we measure is a location parameter. In the remainder of this section, we focus on the presented acceleration sensor, but our reasoning extends to other ΔΣ systems as well because the output of the second (or even the first) integrator always are of location-parameter nature.

The smallest quantization interval of our ADC has a width of 15.4mV (it is located in the centre of the input range). This is even larger than the interval of a linear 7-bit quantizer, 1.8V / 27 = 14.1mV, as it would be needed to build a semi-uniform quantizer like the one in [11], and it is much larger than the very small quantization steps used in the centre range of μ-law ADCs [10]. Note that this quantizer is built for an input distribution that has a specific standard deviation. The stage preceding it must therefore be a programmable-gain amplifier whose gain can be set differently for different applications and sensors. In our system, it is programmable in the range 10−230.

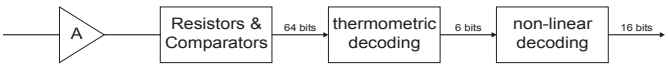

Figure 5. Non-linear ADC block diagram.

The schematic of our ADC is shown in Figure 5. It consists of a block containing comparators and a resistive divider, similar to a flash ADC, but constructed with non-linearly distributed decision thresholds. The output is a thermometric code from which the number of the quantization interval is calculated. Finally, a look-up table (in our test setup residing on an FPGA) computes the output with a precision of 16 bits, which is the input format required for the digital filter block.

D. Digital Filter

The ΔΣ loop further includes an external 3rd-order digital filter with a fixed-point implementation and configurable coefficients. The latter can be adjusted in order to preserve the overall loop stability and optimize the noise spectrum for a wide range of MEMS sensors. The function implemented is a 3rd-order integrator, combined with a zero used to compensate for the phase shift due to the 2nd-order integrating function of the sensor in order to achieve loop stability.

The output of the digital filter determines the direction in which the actuation force is applied. It is noteworthy that the 1-bit quantizer used in this ΔΣ loop is a digital one. From the fixed-point calculation of the filter output, only the sign is kept to determine the digital output of the system (bitstream) and the direction of the actuation on the sensor (force).

IV. Measurement Results

The complete mixed-signal front end has been integrated in a 0.6μm CMOS process with HV options. The ASIC includes the HV switches, the analog front end with the preamplifier, the CDS demodulators, and the 7-bit flash ADC. The digital filter was implemented in an FPGA, and a Colibrys low-noise MEMS sensor (mass: 3.5mg; noise: 0.8μg/√Hz) was connected to the ASIC through shielded wires and a printed circuit board (PCB).

The system has a full scale of 11g and a bandwidth of 300Hz. Figure 6 shows the measured normalized output spectrum of the ΔΣ loop without excitation in an environment with a very low level of acceleration noise. The noise floor is at 1.15μg/√Hz, which corresponds to a dynamic range (DR) of 19 bits over the 300-Hz bandwidth.

Figure 7 shows the result when an 8-g excitation at 222Hz is applied. The shaker table used in this measurement stood in a room with higher gravitation noise in the frequency range 20-60Hz. The noise figure measured in that room is identical if no signal is applied by the shaker. The signal harmonics that can be seen correspond to the non-linearity of the shaker, which has been verified by measurements using a different high-precision low-noise reference accelerometer. For the 8-g sinusoidal acceleration at 222Hz, the measured white-noise floor goes up to 7.1μg/√Hz in the signal band, corresponding to an SNR of 16 bits.

The DR that is 3 bits higher than the SNR is particularly interesting for inertial navigation applications, where the noise performance at reduced signal level is important. Further characteristics and measurement results are presented in Table I. The system features 2.3b higher SNR and 5.2b higher DR than [14] when normalized to the same bandwidth.

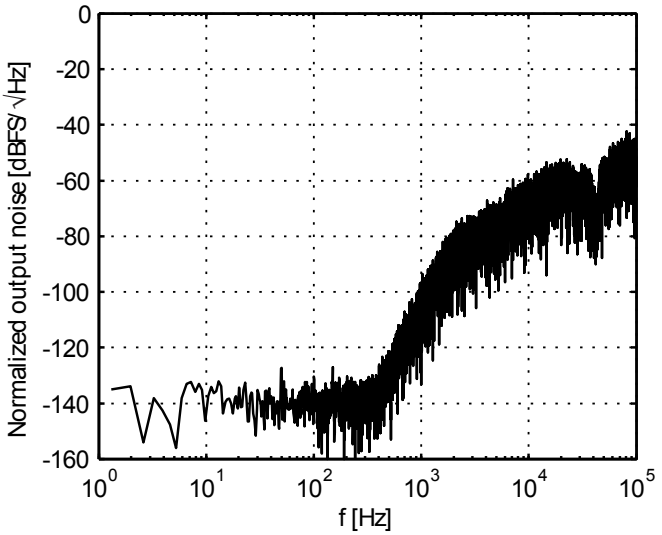

Figure 6. Normalized output noise spectrum without excitation.

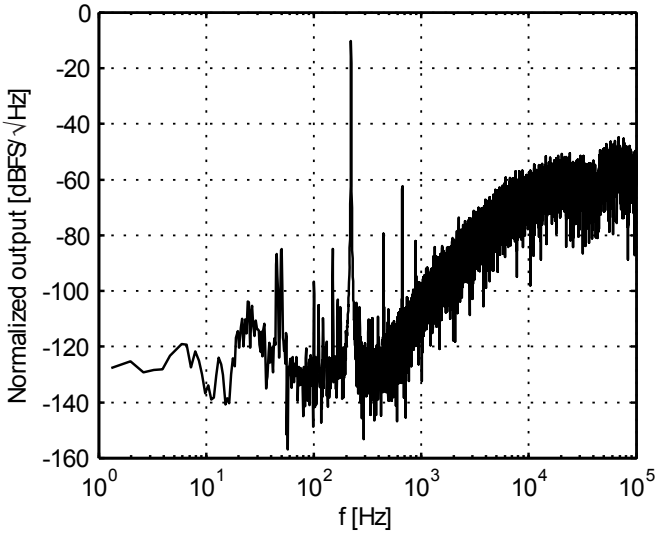

Figure 7. Normalized output noise spectrum with an 8g sinusoidal excitation at 222Hz.

TABLE I. SYSTEM CHARACTERISTICS AND PERFORMANCES

Parameter	Value	Unit
Supply voltage (LV)	3.3	V
Supply voltage (HV)	± 9	V
Power consumption	40	mW
Sampling frequency	1	MHz
Loop order	2 (sensor) + 3 (digital) = 5	-
Analog front-end gain	10-230	-
Preamplifier input noise	10	nV/√Hz
Signal bandwidth	300	Hz
Full scale	11.7	g
Input noise (no signal)	1.7	µg/√Hz
Dynamic range (300Hz BW)	19	bits
Input noise (full-scale signal)	7.1	µg/√Hz
Signal-to-noise ratio (300Hz BW)	16	bits
Chip area	9.7	mm^2

TABLE II. PERFORMANCE REVIEW

Parameter	This work	QA 2030	Unit
Full scale	11.7	60	g
Noise	1.7	3	µg/√Hz
Dynamic range (1Hz BW)	22.2	24.2	bits
Bandwidth	300	500	Hz
Bias stability (24h)	0.1	0.1	mg
Non-linearity (K2)	<10	<20	$µg/g^2$
Bias temperature coefficient	100	<30	µg/°C
Scale-factor temperature coefficient	75	180	ppm/°C

Table II further compares the performance with an industry standard, the Honeywell Q-Flex 2000-030 [16]. For inertial applications, the bias stability, non-linearity and temperature stability are essential features [15].

Bias stability performance is presented in Figure 8, along with the temperature evolution during the measurement, which explains part of the drift observed. The measurement over one hour shows a bias drift of less than ±12µg over a 10g dynamics, i.e. well below ±10ppm. This makes this sensor well suitable for navigation grade inertial sensing applications.

The bias shift induced by vibration and shifted to DC through sensor nonlinearity (dominated by second harmonic K2), called vibration rectification error (VRE), is an important parameter for inertial navigation.

Extremely low K2 non-linearity values $<10µg/g^2$ are measured [15]. However, due to the servo-loop operation and excellent linearization capability of the electrostatic forces through ΔΣ control, K2 is expected to be below $1µg/g^2$. Reported values are still limited by measurement capabilities and not system performance.

Finally, preliminary temperature characterizations from −30°C to +80°C show a temperature dependence of the bias as low as 100µg/°C, and a typical K1 scale factor <75ppm/°C.

Figure 9 presents a micrograph of the ASIC. The total area is $9.7mm^2$. The HV switches occupy $1.1mm^2$, the analog circuit $0.6mm^2$, and the ADC $0.4mm^2$. The area occupied by the digital configuration and control block is needed only for testing this prototype. The ASIC power consumption (preamplifier, CDS, ADC and switch control logic) is 40mW.

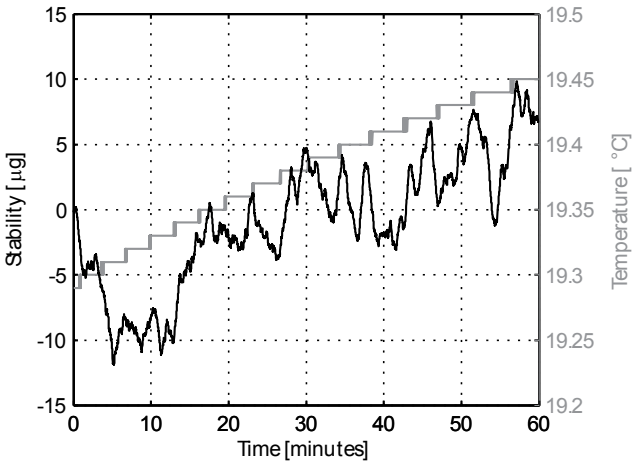

Figure 8. Bias stability measurement.

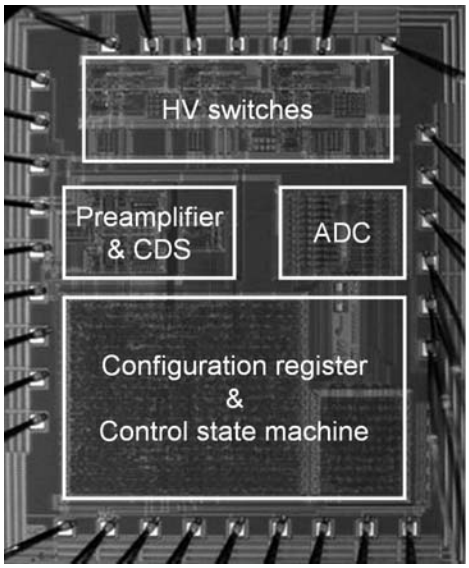

Figure 9. Circuit micrograph.

V. CONCLUSION

The accelerometer front-end presented in this paper is generic and allows interfacing a wide range of sensors. It consists of HV switches for driving the MEMS, a low-noise preamplifier, a set of demodulators for CDS, and a 7-bit flash ADC. The gain of the circuit can be programmed to accommodate for sensor characteristics. An external reconfigurable 3rd-order digital filter is used to raise the total loop order to 5 and thus improve the system resolution. This mixed-signal ΔΣ loop implementation and its programmable filter can interface MEMS sensors to realize accelerometers in the sub-g to 100g range with high linearity and very good noise performance. With a Colibrys low-noise MEMS sensor, the system exhibits a 19-bit dynamic range and 16-bit SNR over the 300Hz signal bandwidth.

ACKNOWLEDGMENT

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