A 300Hz 19b DR Capacitive Accelerometer based on a Versatile Front End in a 5th-order ΔΣ Loop

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***Abstract*—This paper presents a 5th-order ΔΣ capacitive accelerometer. The ΔΣ loop is implemented in mixed signal, the global 5th-order filter having a 2nd-order analog and a 3rd-order digital part. The system can be used with a wide range of sensors, because the mixed-signal front end is programmable. The ASIC developed comprises a voltage-mode preamplifier, two parallel demodulators implementing CDS, and a 7-bit Flash ADC. The latter drives a 3rd-order digital filter, which can be configured for different sensor parameters in order to ensure overall loop stability and optimize the noise performance. With a low-noise MEMS sensor, the system achieves a 19-bit DR and a 16-bit SNR, both over a 300Hz bandwidth.**

I. Introduction

Micro-electro-mechanical systems (MEMS) accelerometer sensors embedded in closed-loop ΔΣ ADCs achieve high performances. The high resolution and precision of these systems [1][2] allow their use in demanding applications like inertial navigation or seismic measurements. Different sensor designs address the specific needs of each application. There is thus a need for an electronic front end that can adapt to a wide range of sensors characteristics without needing to be redesigned, and that still achieves very high resolutions.

This paper presents such a generic accelerometer system that can be reconfigured. It consists of an application-specific integrated circuit (ASIC) containing a versatile analog front end, a low-precision ADC and an external digital filter.

II. System Architecture

Figure 1 presents the architecture of the accelerometer system. The capacitive accelerometer MEMS sensor is a moving mass in the middle between two fixed plates. These three electrodes are connected to a set of high-voltage (HV) switches that apply actuation and position sensing pulses. An additional HV switch connects the middle electrode to the low-voltage (LV) preamplifier in the analog front end during position sensing, and protects the LV circuit during HV actuation of the middle electrode. The analog front end ASIC is a high-speed low-precision position measurement interface consisting of a low-noise voltage-mode preamplifier, demodulators for correlated double sampling (CDS) and a 7-bit Flash analog-to-digital converter (ADC). The gain of each block is configurable to fit the sensor characteristics.

Since the sensor already integrates the input and feedback signals of the ΔΣ loop twice, the requirement on the analog front end precision is relaxed: 7-bit precision gives sufficiently good noise and distortion performance for all the different sensors to be used with the system. The digitized output is fed into a 3rd-order digital filter that increases the loop order to five, giving the system a high resolution. Finally, the sign of the output of the digital filter, which is the output bitstream, also determines the direction in which the actuation force is applied to the sensor.

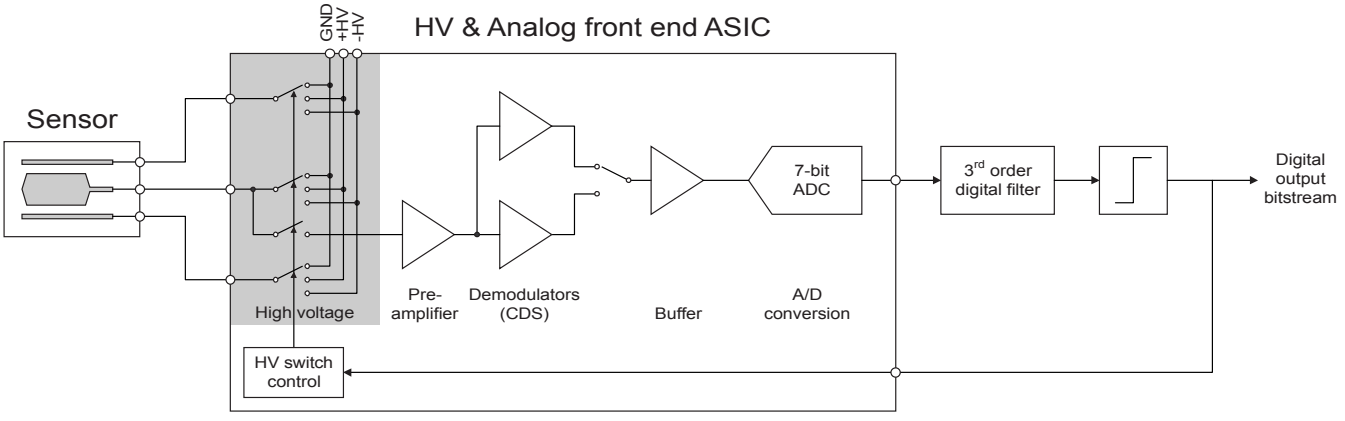

Figure 1. System architecture.

III. SENSOR AND FRONT END

The sensor and its interface comprising the HV switches and the preamplifier from Figure 1 are detailed in Figure 2. The HV-switch control signals are shown for a typical operating cycle. The 1µs cycle period is subdivided into one position-sensing phase and one actuation phase which are equal in length (0.5µs each). The electrostatic actuation force is generated by connecting the moving mass and one plate to one of the HV supplies, and the second plate to the opposite HV supply.

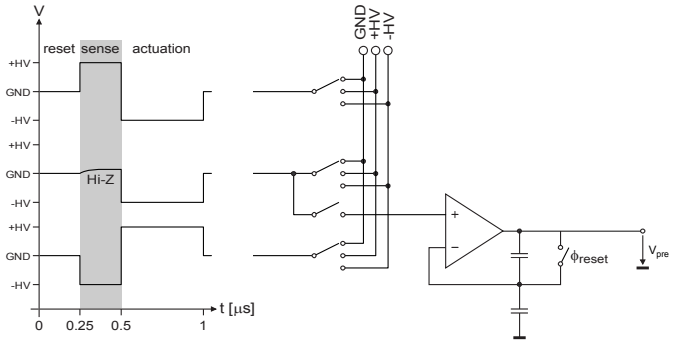

Figure 2. Sensor and analog front end.

The position-sensing phase starts by short-circuiting the three sensor electrodes to ground in order to discharge the sensor capacitances (reset). Then the two fixed electrodes are connected to the positive and negative HV supplies, and the moving-mass electrode is connected to the high-impedance input of the preamplifier. Since the sensor capacitance values reflect the position of the moving mass, the middle point of the sensor capacitive bridge displays a corresponding voltage variation. If $C_t(x)$ is the capacitance between the top plate and the middle electrode, $C_b(x)$ the one between the bottom plate and the middle electrode, and x the distance of the moving mass to its equilibrium point in the middle between the electrodes, the middle electrode voltage V_{mid} during the sense phase depicted in Figure 2 is:

$$V_{mid}(x) = -HV + 2HV\frac{C_t(x)}{C_t(x)+C_b(x)} \qquad (1)$$

Since the feedback control loop tries to keep the moving mass in the middle between the top and bottom plates, the displacement of the mass is so small that $C_t(x)$ and $C_b(x)$ vary linearly and symmetrically with a C_Δ sensitivity around a nominal value C_0:

$$C_t(x) = C_0 + C_\Delta \cdot x \quad ; \quad C_b(x) = C_0 - C_\Delta \cdot x \qquad (2)$$

Equation (1) then simplifies to:

$$V_{mid}(x) = HV \cdot \frac{C_\Delta}{C_0} \cdot x \qquad (3)$$

This voltage is amplified by the voltage-mode preamplifier with a capacitive feedback, which is reset prior to amplification. The sign of the output signal can be reversed by exchanging the positive and negative HV supply connections to the top and bottom plates (+sense and -sense in Figure 3), which then allows to perform CDS as discussed in the next section.

The gain of the voltage-mode preamplifier stage is fixed by a capacitor ratio and does not depend on the sensor capacitance value, as it does in charge-mode amplifier topologies [3]. This allows setting the gain of the preamplifier precisely. A low gain value of 10 is chosen to achieve accurate settling within 250ns. A second advantage of the voltage amplifier is that, unlike the charge amplifier, it does not accelerate the sensor mass during read-out, which gives higher linearity. Finally, the noise performance is also increased by using the voltage-mode approach [4].

IV. DEMODULATION & CDS

Figure 3 shows one demodulator circuit implementing the CDS, as well as the corresponding switch control signals.

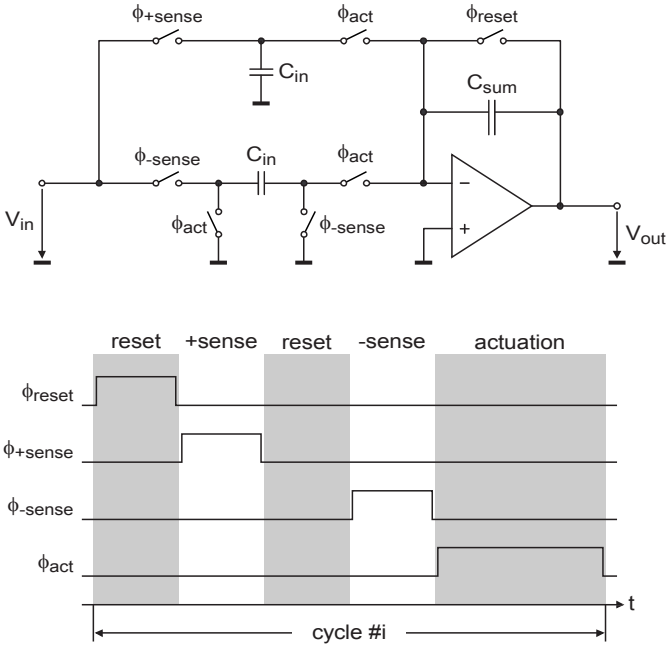

Figure 3. Demodulator and CDS implementation.

The circuit subtracts the pre-amplified signals resulting from two successive +sense and -sense phases during the same cycle, which has the effect of cancelling the offset and 1/f noise of the preamplifier.

The signal is sampled directly on the input capacitors at the end of each sense phase. The charge is then transferred to the summing capacitor during the actuation phase, allowing 500ns for the amplifier to settle and thus relaxing its gain-bandwidth (GBW) design constraints. To accommodate for different sensor characteristics, the gain of the demodulator can be programmed by adjusting the feedback capacitor (C_{sum}). Since the necessary precision of 7 bits is moderate, a parasitic-sensitive circuit can be used.

The disadvantage of the scheme presented in Figure 3 is that because there are two reset and sense phases, the cycle becomes longer. To overcome this limitation, the two sense phases needed for CDS can be part of two successive cycles. There is then only one reset and sense phase per cycle, the +sense and –sense being alternated from cycle to cycle. However, the demodulation output can then calculated only every second cycle, which reduces the ΔΣ loop frequency and decreases performance.

It is also possible to implement the scheme of Figure 4, which uses two demodulators in a time-interleaved fashion. Then each cycle contains either a +sense or a –sense phase. When the first demodulator is performing its first demodulation operation, the second demodulator already finishes the second one and the value computed is fed out. During the next cycle, the roles are reversed and so on. In this way, there is one output value for each cycle without needing two sense phases per cycle or increasing the cycle length. Compared to Figure 3, only one cycle of excess loop delay remains. The optimum choice of the CDS scheme to use depends both on the sensor used, the required signal bandwidth and the noise performance expected.

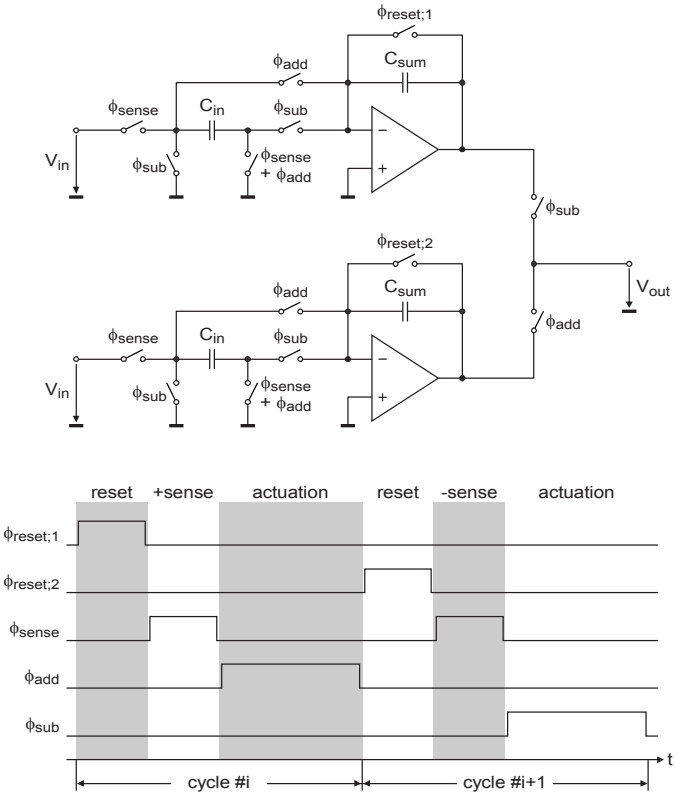

Figure 4. Time-interleaved CDS using 2 demodulators.

V. Analog to Digital Conversion & Filtering

The output of the analog front end is digitized by a low-precision ADC, which is also integrated in the ASIC. The speed and precision requirements are the same as for the analog circuit, i.e. 1MS/s with 7-bit precision. A Flash implementation is used.

The ΔΣ loop further includes an external 3rd-order digital filter with a fixed-point implementation and configurable coefficients. The latter can be adjusted in order to preserve the overall loop stability and optimize the noise spectrum for a wide range of MEMS sensors. The function implemented is a 3rd-order integrator, combined with a zero used to compensate for the 2nd-order integrating function of the sensor in order to achieve loop stability.

The output of the digital filter determines the direction in which the actuation force is applied. It is noteworthy that the 1-bit quantizer used in this ΔΣ loop is a digital one. From the fixed-point calculation of the filter output, only the sign is kept to determine the digital ouptut of the system (bitstream) and the direction of the actuation on the sensor (force).

VI. Measurement Results

The complete mixed-signal front end has been integrated in a 0.6μm CMOS process with HV options. The ASIC includes the HV switches, the analog front end with the preamplifier and the CDS demodulators, and the 7-bit Flash ADC. The digital filter was implemented in an FPGA, and a Colibrys low-noise MEMS sensor (mass: 3.5mg; noise: 0.8μg/√Hz) was connected to the ASIC through shielded wires and a printed circuit board (PCB).

The system has a full scale of 11g and a bandwidth of 300Hz. Figure 5 shows the measured normalized output spectrum of the ΔΣ loop without excitation in an environment with a very low level of acceleration noise. The noise floor is at 1.15μg/√Hz, which corresponds to a dynamic range (DR) of 19 bits over the 300Hz bandwidth.

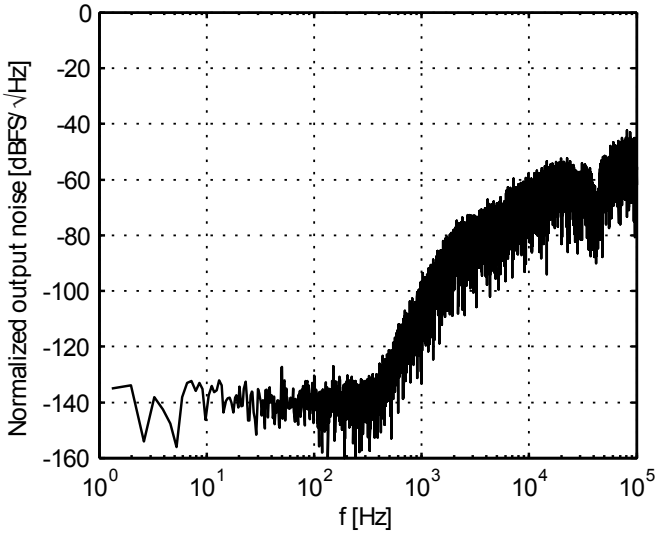

Figure 5. Normalized output noise spectrum without excitation.

Figure 6 shows the result when an 8g excitation at 222Hz is applied. The shaker table used in this measurement stood in a room with higher gravitation noise in the frequency range 20-60Hz. The noise figure measured in that room is identical if no signal is applied by the shaker. The signal harmonics that can be seen correspond to the non-linearity of the shaker, which has been verified by measurements using a different

high-precision low-noise reference accelerometer. For the 8g sinusoidal acceleration at 222Hz, the measured white-noise floor goes up to 7.1μg/√Hz in the signal band, corresponding to an SNR of 16 bits.

The DR that is 3 bits higher than the SNR is particularly interesting for inertial navigation applications, where the noise performance at reduced signal level is important. Further characteristics and measurement results are presented in Table I. The system features 2.3b higher SNR and 5.2b higher DR than [1] when normalized to the same bandwidth.

Figure 7 presents a micrograph of the ASIC. The total area is 9.7mm^2. The HV switches occupy 1.1mm^2, the analog circuit 0.6mm^2, and the ADC 0.4mm^2. The area occupied by the digital configuration and control block is needed only for testing this prototype. The ASIC power consumption (preamplifier, CDS, ADC and switch control logic) is 12mW.

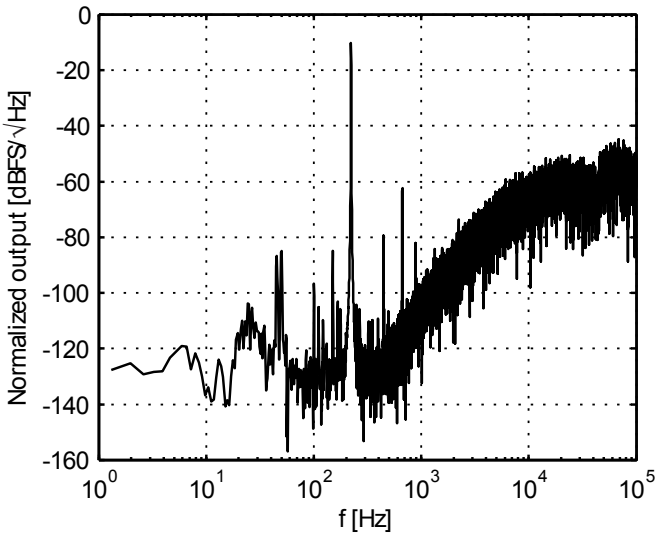

Figure 6. Normalized output noise spectrum with an 8g sinusoidal excitation at 222Hz.

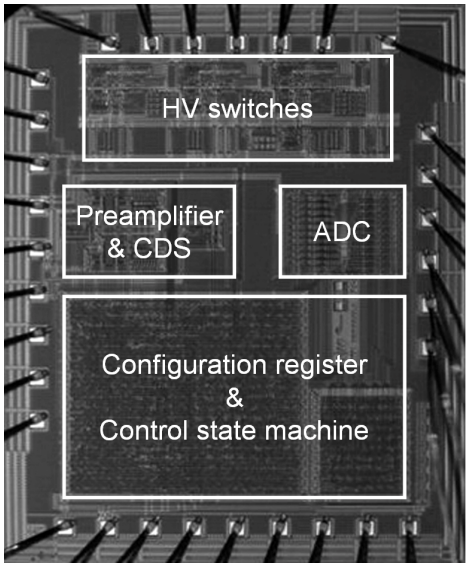

Figure 7. Circuit micrograph.

TABLE I. SYSTEM CHARACTERISTICS AND PERFORMANCES

Parameter	Value	Unit
Supply voltage (LV)	3.3	V
Supply voltage (HV)	± 9	V
Power consumption	12	mW
Sampling frequency	1	MHz
Loop order	2 (sensor) + 3 (digital) = 5	-
Analog front end gain	10-230	-
Preamplifier input noise	10	nV/√Hz
Signal bandwidth	300	Hz
Full scale	11	g
Input noise (no signal)	1.15	μg/√Hz
Dynamic range (300Hz BW)	19	bits
Input noise (full-scale signal)	7.1	μg/√Hz
Signal-to-noise ratio (300Hz BW)	16	bits
Chip area	9.7	mm^2

VII. CONCLUSION

The accelerometer front end presented in this paper is generic and allows interfacing a wide range of sensors. It consists of HV switches for driving the MEMS, a low-noise preamplifier, a set of demodulators for CDS, and a 7-bit Flash ADC. The gain of the circuit can be programmed to accommodate for sensor characteristics. An external reconfigurable 3rd-order digital filter is used to raise the total loop order to 5 and thus improve the system resolution. This mixed-signal ΔΣ loop implementation and its programmable filter can interface MEMS sensors to realize accelerometers in the sub-g to 100g range with high linearity and very good noise performance. With a Colibrys low-noise MEMS sensor, the system exhibits a 19-bit dynamic range and 16-bit SNR over the 300Hz signal bandwidth.

ACKNOWLEDGMENT

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