CIRCUIT TRANSPOSITION USING SIGNAL-FLOW GRAPHS

Hanspeter Schmid

Bernafon AG, Morgenstrasse 131, 3018 Bern, Switzerland. E-mail: h.p.schmid@ieee.org

ABSTRACT

This paper proves the circuit transposition theorem using signal-flow graphs (SFGs). The proof has two advantages: it is constructive, and it is intuitive for engineers who know SFGs. For these engineers, our technique makes it easy to derive the dual counterpart of any amplifier and enables them to transpose all linear circuits without resorting to the circuit transposition tables that were published in many other papers. Because the main purpose of this paper is to provide a tool for analog circuit analysis and design, the proof is written in tutorial style.

1. INTRODUCTION TO CIRCUIT TRANSPOSITION

A linear circuit Ξ can always be described by two frequency-domain equations,

$$\mathbf{A}\mathbf{x} = \mathbf{b}U \tag{1}$$

$$Y = \mathbf{c}^{\mathrm{T}}\mathbf{x} \tag{2}$$

where U is the input signal and Y is the output signal. $\mathbf{A}$ is the $(m+n)\times(m+n)$-dimensional matrix that contains the coefficients of a complete set of linearly independent network equations describing Kirchhoff's current law at n different nodes and Kirchhoff's voltage law around m different loops. $\mathbf{x}$ is an $m+n$-dimensional vector of independent network variables. Vector $\mathbf{b}$ indicates how the input signal is connected to the network, and $\mathbf{c}$ describes how the output signal is derived from the network. Normally, all of them are functions of s, so we omit s for reasons of brevity. The transfer function of Ξ is then

$$T(s) = \frac{Y(s)}{U(s)} = \mathbf{c}^{\mathrm{T}}\mathbf{A}^{-1}\mathbf{b}\,. \tag{3}$$

The operation of replacing $\mathbf{A}$ by $\mathbf{A}^{\mathrm{T}}$ and swapping $\mathbf{b}$ and $\mathbf{c}$ is called *circuit transposition*. The new circuit Ξ_{t} is *dual* to Ξ. It has the transfer function

$$T_{\mathrm{d}} = \frac{Y_d}{U_d} = \mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c}\,. \tag{4}$$

T_{d} can be interpreted as a 1×1 matrix and can be transposed like any other matrix. Trivially, 1×1 matrices are not changed by transposition; thus the following derivation can be made:

$$\begin{aligned} T_{\mathrm{d}} = {T_{\mathrm{d}}}^{\mathrm{T}} &= \mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c} = \left(\mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c}\right)^{\mathrm{T}} \\ &= \mathbf{c}^{\mathrm{T}}\left(\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\right)^{\mathrm{T}}\mathbf{b} = \mathbf{c}^{\mathrm{T}}\mathbf{A}^{-1}\mathbf{b} = T\,. \end{aligned} \tag{5}$$

Therefore the transfer function of the dual circuit and the transfer function of the original circuit are identical.

Up to here, the discussion was only an exercise in linear algebra, but the most important question has been left unanswered: what does it actually mean for a circuit if $\mathbf{A}$ is replaced by $\mathbf{A}^{\mathrm{T}}$ and $\mathbf{b}$ and $\mathbf{c}$ are exchanged? To answer this question, it is necessary to specify $\mathbf{x}$ more precisely. In the literature, $\mathbf{x}$ typically consists of all node voltages and several branch currents. It can then be shown by matrix algebra how a concrete circuit can be transposed, either directly [1] or by way of so-called intermediate transfer functions [2, 3]. An alternative way to show how a circuit must be transposed is to start with the more general concept of adjoint circuits [4], which also deals with non-linear circuits, and of which linear circuit transposition is just a special case.

These proofs are un-intuitive for most engineers and engineering students, because abstract network theory is scarcely taught anymore. Today, circuit transposition is often explained by stating that the passive part of the network does not change and by giving transposition tables for the active elements in the circuit (c.f. [1, 5–7]). It is demonstrated in this paper how the whole problem can be tackled using signal-flow graphs. This has the advantage that the concept of circuit transposition becomes intuitive for all engineers who have some understanding of signal-flow graphs (SFGs) or feedback block diagrams.

In the following, we will first introduce the so-called *driving-point signal-flow graphs* (DP SFGs). Then we will define SFG transposition and show how the circuit corresponding to a transposed SFG can be derived. Finally, we will show that transposing the DP SFG of a circuit really is the same as transposing the circuit itself.

2. DRIVING-POINT IMPEDANCES AND SIGNAL-FLOW GRAPHS

A new technique to analyse linear networks was presented recently, which combines driving-point impedance analysis with signal-flow graph (SFG) analysis [8]. We will now explain this technique by using an example, but in a different way than it was explained in [8].

Fig. 1 shows an active-RC low-pass filter, consisting of four passive elements, R_1, R_2, C_1, and C_2, and one active element, a voltage amplifier with gain α_{V}. Its nodes are numbered from **1** to **4**. Driving-point analysis, as presented in [8], bases on the following simple observation: If a voltage source is connected to node j and its voltage V_j is set such that no current flows through the source, then nothing changes. This condition can also be expressed in terms of V_j: If a voltage source is connected to node j, and if its voltage V_j is set to the node voltage the circuit had before the source was connected, nothing changes. Note that these auxiliary sources are essentially *controlled* sources, since the appropriate

The main part of work that lead to this publication was done while the author was a doctoral student at the Federal Institute of Technology (ETH) Zürich, Switzerland.

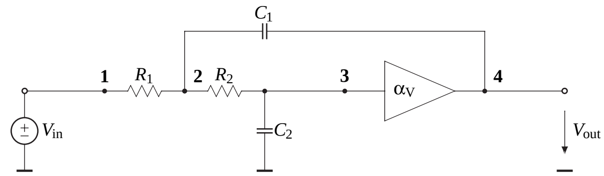

Figure 1: Voltage-mode Sallen-and-Key lowpass filter

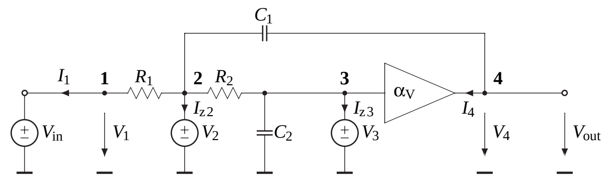

Figure 2: The same filter with auxiliary sources

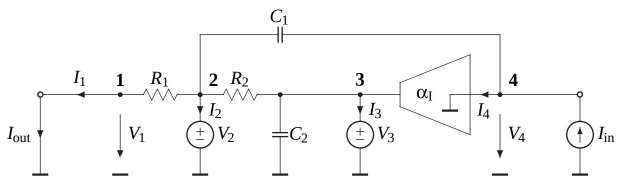

Figure 3: Current-mode filter

V_j depends on the input signal. Nevertheless, the source superposition theorem is still valid for these special controlled voltage sources, since they are chosen explicitly such that they have no influence whatsoever on the circuit. A formal proof of this statement expresses the same idea mathematically to show that the superposition conditions [9] still hold; it is omitted here for reasons of brevity.

In order to obtain a complete set of node voltages and associated branch currents, one current must be assigned to every node voltage. For the nodes with zero node impedance, i.e., the nodes to which a voltage source or a current sink is connected, the current through the voltage source or current sink is chosen. Auxiliary voltage sources are connected to all nodes with non-zero node impedance, e.g., the nodes **2** and **3** in Fig. 1.

Fig. 2 shows the filter with auxiliary voltage sources connected to the nodes **2** and **3**. Since voltage sources are now present at all nodes, applying the source superposition theorem is a straightforward procedure. For example, the current flowing into the auxiliary source 2 can be expressed as

$$I_{z2} = V_1 \cdot \frac{1}{R_1} - V_2 \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} + sC_1 \right) + V_3 \cdot \frac{1}{R_2} + V_4 \cdot sC_1 \ . \quad (6)$$

By definition of the auxiliary sources, $I_{z2} = 0$. If we denote the sum of currents contributed by all voltage sources but source 2 as I_2, then equation (6) can be rewritten as follows:

$$V_2 = I_2 \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} + sC_1 \right)^{-1} = I_2 \cdot Z_2$$
$$\text{with} \quad I_2 = V_1 \cdot \frac{1}{R_1} + V_3 \cdot \frac{1}{R_2} + V_4 \cdot sC_1 \ . \quad (7)$$

Z_2 is called the *driving-point impedance* at node **2** under the condition that all sources but source 2 are set to zero.

Equation (7) can directly be drawn in form of a signal-flow graph, shown in Fig. 4. It is obvious from the derivation above how the branches “belonging” to the auxiliary source connected to node j are formed:

1. There is one branch from I_j to V_j. Its weight is Z_j, the driving-point impedance at node k under the condition that $V_k = 0$ for all $k \neq j$.
2. For each node k, with $k \neq j$, there is a branch from V_k to I_j if and only if the two nodes are directly connected by a component. If this is so, the weight of the branch is the admittance of the connecting component.

This procedure can easily be repeated for the auxiliary source 3, as shown in Fig. 5.

It is still necessary to describe the amplifier, and how the input source and the filter output are connected to the circuit:

$$V_4 = \alpha_V V_3 \ , \quad V_1 = V_{in} \ , \quad V_{out} = V_4 \ . \quad (8)$$

The result is shown in Fig. 6. It appears that the variables I_1 and I_4 are not used at all, but it is good from a didactic point of view to include them into the signal-flow graph.

Note that the signal-flow graph in Fig. 6 has two loops. It is also possible, using a different technique, to directly derive a signal-flow graph for the filter in Fig. 1 which has only one loop [7]. Then Mason’s gain rule is easier to apply. However, the technique presented here has two great advantages: it can be applied to *any linear circuit* (it is especially easy to apply it to Gm–C filters), and it can be applied *mechanically*. This makes it possible to use it for deriving dual circuits.

3. TRANSPOSITION OF SIGNAL-FLOW GRAPHS

In this section, all the rules for transposing circuits are derived using only the driving-point signal-flow graph described in the previous section. The only element of signal-flow graph theory required for the proof is Mason’s gain rule, which he introduced in [10] and proved in [11], and which can be found in any textbook covering signal-flow graphs. It is, in Mason’s notation:

$$G = \frac{\sum_k G_k \Delta_k}{\Delta} \ . \quad (9)$$

Δ is called the graph determinant. It is of the form

$$\Delta = 1 - S_1 + S_2 - S_3 + \dots \ , \quad (10)$$

where S_1 is the sum of all loops, S_2 is the sum of all products of two loops without common nodes, and S_j is the sum of all products of j loops without common nodes. G_k is the gain of the k-th forward path, and Δ_k is the part of the graph determinant which contains only loops that do not have nodes in common with the path G_k. What G actually is depends on the signal-flow graph in question. For example, the gain of the signal-flow graph in Fig. 6 is $G = V_{out}/V_{in}$, which is the voltage transfer function T of the circuit in Fig. 1.

It can be tedious to evaluate this gain formula for larger circuits, but for our purpose it is enough to note the following: Two graphs have the same gain G if

1. they have the same forward paths,
2. they have the same loops,

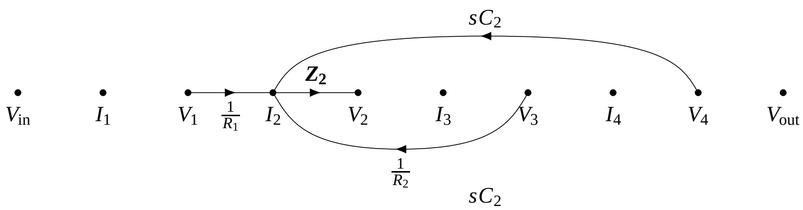

Figure 4: Equation (7) drawn as a signal-flow graph

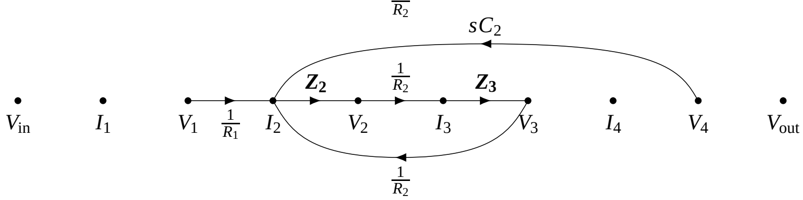

Figure 5: Signal-flow graph branches "belonging" to the two auxiliary sources

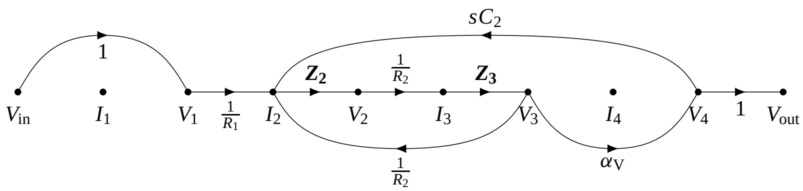

Figure 6: Complete signal-flow graph of the circuit in Fig. 2

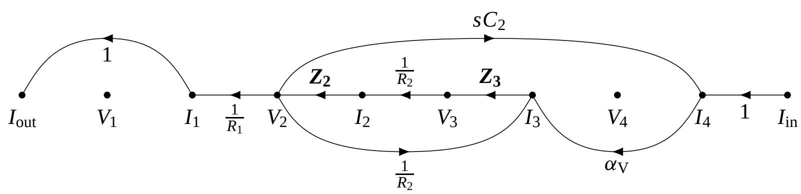

Figure 7: Transposed signal-flow graph describing the circuit in Fig. 3

3. the topological relations (i.e. common nodes) between the loops and between loops and forward paths are the same.

When the directions of all branches of a signal-flow graph are reversed, the forward paths and loops as well as the topological relations between them remain unchanged. Therefore the SFG gain also remains the same. We call this operation the *transposition of a signal-flow graph* and the SFG resulting from it the *dual* SFG. For example, this means that the graph in Fig. 7 has the same gain as the dual graph in Fig. 6. Note that nodes formerly describing voltages describe currents in the dual graph, and vice versa. This is necessary since the branch weights are not changed, and, e.g., an admittance branch must still originate from a voltage node and lead into a current node. Therefore $G_d = I_{\text{out}}/I_{\text{in}}$, which means that the circuit corresponding to the dual graph in Fig. 7 has the *current* transfer function T. It actually is the dual circuit, which will be shown presently.

3.1. Transposition of the example

To find out what the circuit described by the signal-flow graph in Fig. 7 looks like, we first note that the new circuit has the same number of nodes. First to the passive branches: The driving-point impedances are still present at the same nodes as before the transposition. The admittance branch from V_j to I_k is now leading from V_k to I_j. Thus the admittances between the nodes do not change either if the circuit is transposed. *The passive part remains the same.*

The input voltage source is replaced by a current output, the voltage output by an input current source. Finally, the gain α_V now points from I_4 to I_3: the voltage amplifier is replaced by a current amplifier with a gain of the same absolute value. Note that the current direction *into* the output of a current amplifier is conventionally considered to be positive, but the branch with weight α_V actually contributes a current into the auxiliary source at node **3**, which flows *out* of the current amplifier, which therefore has a gain of $\alpha_I = -\alpha_V$. The resulting circuit is shown in Fig. 3.

3.2. Derivation of transposition rules

The same method can also be applied to only a part of a circuit, e.g. a single active element: First, the signal-flow graph of the element is drawn, then it is transposed, and finally the active device described by this signal-flow graph is drawn.

Take, for example, the differential difference operational amplifier (DDOA) in Fig. 8 (c.f. [12, 13]). It amplifies the difference of two voltage differences. The transpose derived in Fig. 8 is a balanced current opamp with mirrored outputs. Again, since we define positive currents as flowing *into* the output of an active device, but the signal-flow-graph current is defined as flowing *out of* the output of the active device, the signs of the current opamp outputs are the inverse of the signs of the DDOA inputs.

A second example is the operational floating conveyor (OFC). It works as follows: the voltage applied to terminal Y is copied to terminal X. The current flowing into this terminal is then amplified by a very high transresistance r_m, which gives a voltage at terminal W. Finally, the current flowing into terminal W is copied to flow out of terminal Z. From this description, the signal-flow graph of the device follows immediately, but it is important to choose the current directions correctly. The terminals X and W are a current sink and a voltage source, respectively, so I_2 and I_3 are positive if they flow into the OFC. On the other hand, terminals Y and Z are high-impedance terminals, to which either a current sink, a voltage

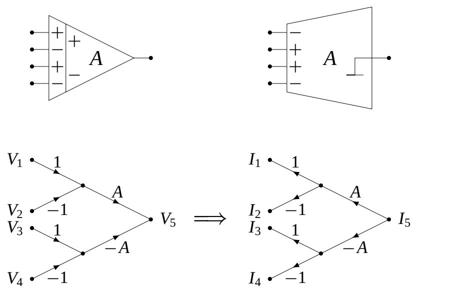

Figure 8: Differential difference opamp.

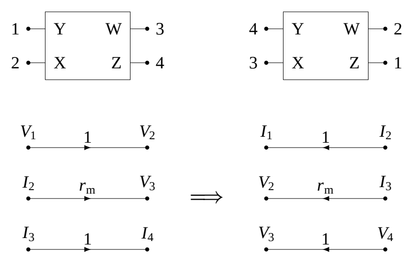

Figure 9: Operational floating conveyor.

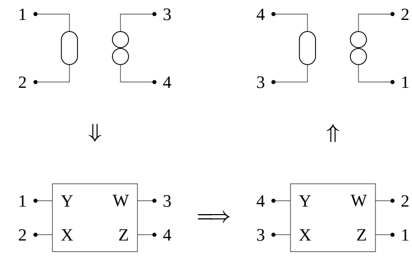

Figure 10: Nullor.

source, or an auxiliary source is connected. In any of these three cases, I_1 and I_4 are positive if they flow out of he OFC. Note that the transpose of this signal-flow graph is identical to the original one. Thus the operational floating conveyor is its own transpose, only the terminals are permuted during transposition, as indicated by the numbers in Fig. 9. The same is true for other devices, e.g. the balanced-output OTA and the negative-gain second-generation current conveyor (CCII−), but these proofs are left to the reader.

One more example: as discussed in [12], the OFC with $r_m \to \infty$ approximates a four-terminal nullor. Thus the OFC can be used to show that the nullor can be transposed by interchanging nullator and norator, as shown in Fig. 10. The same could, of course, also be done by using the balanced-output OTA with $g_m \to \infty$.

4. SFG TRANSPOSITION AND CIRCUIT TRANSPOSITION

We have not yet proved that SFG transposition is the same as circuit transposition. In general, this is not necessarily the case, but it is the case for DP SFGs. The proof is straightforward: the voltages and currents of all nodes occur in the signal vector,

$$\mathbf{x}^{\mathrm{T}} = \begin{bmatrix} V_1 & V_2 & V_3 & V_4 & I_1 & I_2 & I_3 & I_4 \end{bmatrix}. \qquad (11)$$

Then the coefficient matrix can be built by writing down the DP SFG equations in a systematic way: first the equation describing the nodes V_1 to V_4, then the equations describing the nodes I_1 to I_4.

$$\mathbf{A} = \begin{bmatrix} y_{1,1} & y_{1,2} & y_{1,3} & y_{1,4} & -1 & a_{1,2} & a_{1,3} & a_{1,4} \\ y_{2,1} & y_{2,2} & y_{2,3} & y_{2,4} & a_{2,1} & -1 & a_{2,3} & a_{2,4} \\ y_{3,1} & y_{3,2} & y_{3,3} & y_{3,4} & a_{3,1} & a_{3,2} & -1 & a_{3,4} \\ y_{4,1} & y_{4,2} & y_{4,3} & y_{4,4} & a_{4,1} & a_{4,2} & a_{4,3} & -1 \\ -1 & b_{1,2} & b_{1,3} & b_{1,4} & Z_1 & z_{1,2} & z_{1,3} & z_{1,4} \\ b_{2,1} & -1 & b_{2,3} & b_{2,4} & z_{2,1} & Z_2 & z_{2,3} & z_{2,4} \\ b_{3,1} & b_{3,2} & -1 & b_{3,4} & z_{3,1} & z_{3,2} & Z_3 & z_{3,4} \\ b_{4,1} & b_{4,2} & b_{4,3} & -1 & z_{4,1} & z_{4,2} & z_{4,3} & Z_4 \end{bmatrix} \qquad (12)$$

where $a_{i,j}$ is the weight of the SFG branch going from V_j to V_i, $b_{i,j}$ is the weight of the SFG branch going from I_j to I_i, $y_{i,j}$ is the weight of the SFG branch going from V_j to I_i, and $z_{i,j}$ is the weight of the SFG branch going from I_j to V_i. Note that $z_{i,i}$ is just the driving-point impedance Z_i.

It now becomes apparent what transposing **A** means for the DP SFG: any branch that left V_i now enters I_i, any branch that entered V_i now leaves I_i, and so on. This is precisely how the transposition of a signal-flow graph is defined. The effect of interchanging **b** and **c** on the DP SFG can be investigated in a similar way and thus confirms that SFG transposition is in fact the same as circuit transposition.

5. CONCLUSION

In this paper, the driving-point signal-flow graph is used as a tool to transpose networks, but they are also a very efficient and versatile circuit analysis tool which we use in our lectures. [8] explains this important aspect of DP SFGs.

6. REFERENCES

[1] B. B. Bhattacharyya and M. N. S. Swamy, "Network transposition and its application in synthesis," *IEEE Trans. Circ. Theory*, vol. CT-18, no. 3, pp. 394–397, May 1971.

[2] Gordon W. Roberts and Adel S. Sedra, "A generalization of intermediate transfer function analysis to arbitrary linear networks," in *Proc. ISCAS*, Portland, Oregon, May 1989, vol. 2, pp. 1059–1062.

[3] Gordon W. Roberts, "Adjoint networks revisited," in *Proc. ISCAS*, New Orleans, 1990, vol. 1, pp. 540–544.

[4] Stephen W. Director and Ronald A. Rohrer, "The generalized adjoint network and network sensitivities," *IEEE Trans. Circ. Theory*, vol. 16, no. 3, pp. 318–323, Aug. 1969.

[5] Alfonso Carlosena, Sonia Porta, and George S. Moschytz, "Current-mode realization of negative feedback SAB's," in *35th Midwest Symp. Circ. Sys.*, Washington, Aug. 1992, pp. 1296–1299.

[6] Alfonso Carlosena and George S. Moschytz, "Nullators and norators in voltage to current mode transformations," *Int. J. Circ. Theor. Appl.*, vol. 21, no. 4, pp. 421–424, July 1993.

[7] George S. Moschytz and A. Carlosena, "A classification of current-mode single-amplifier biquads based on a voltage-to-current transformation," *IEEE Trans. CAS–II*, vol. 41, no. 2, pp. 151–156, Feb. 1994.

[8] Agustin Ochoa, "A systematic approach to the analysis of general and feedback circuits and systems using signal flow graphs and driving-point impedance," *IEEE Trans. CAS–II*, vol. 45, no. 2, pp. 187–195, Feb. 1998.

[9] Ray R. Chen, Artice M. Davis, and Marwan A. Simaan, "Network laws and theorems," in *The Circuits and Filters Handbook*, Wai-Kai Chen, Ed., chapter 13, pp. 418–474. CRC Press, Inc., Boca Raton, Florida, 1995.

[10] Samuel J. Mason, "Feedback theory — Some properties of signal flow graphs," *Proc. IRE*, vol. 41, no. 9, pp. 1144–1156, Sept. 1953.

[11] Samuel J. Mason, "Feedback theory — Further properties of signal flow graphs," *Proc. IRE*, vol. 44, no. 7, pp. 920–926, July 1956.

[12] Hanspeter Schmid, "Approximating the universal active element," *IEEE Trans. CAS–II*, vol. 47, no. 11, pp. 1160–1169, Nov. 2000.

[13] Eduard Säckinger and Walter Guggenbühl, "A versatile building block: the CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. 22, no. 2, pp. 287–294, Apr. 1987.