A CHARGE-PUMP-CONTROLLED MOSFET–C SINGLE-AMPLIFIER BIQUAD

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ABSTRACT

The spurious-free dynamic range (SFDR) of a MOSFET–C filter can be increased greatly by generating its tuning voltage with a charge pump. In this paper, we apply this technique to build a Sallen-and-Key lowpass filter with a pole frequency of 24 MHz and a pole Q of 3. It has an SFDR better than 50 dB and consumes 16 mW from a 3.3 V supply. Implemented with a double-poly triple-metal 0.6-μm CMOS process, it covers an area of only 0.11 mm^2. In addition to a description of the filter and the charge pump, we also discuss linear and non-linear clock feed-through from the charge pump's own ring oscillator, and derive a formula for the optimum voltage swing at the MOSFET–C network nodes.

1. INTRODUCTION

Most filters used nowadays in the video-frequency range have integrator-connected topologies and are implemented as Gm–C filters or with MOSFET–C integrators. They require at least one amplifier per pole. The use of an active-RC *single-amplifier biquadratic filter, which generates a pair of complex poles using one amplifier only*, reduces both the required chip area and the power consumption. The main problem is that the pole frequency can then only be tuned by adjusting some of the passive components, e.g. the resistors.

The possibility of building active-RC filters in tunable form by implementing the passive part as a MOSFET–C network was first mentioned in [1]. There it was concluded that the most interesting type of single-amplifier filters, the Sallen-and-Key filters, could not be built with a very low distortion. It was recently demonstrated that the moderate-distortion filters used in many video-frequency applications can well be implemented as MOSFET–C Sallen-and-Key filters [2, 3] (see, e.g., the lowpass filter in Fig. 1). Measurements discussed in [2, 3] show that, using a specific current-controlled current source (CCCS), a spurious-free dynamic range (SFDR) of 45 dB is very difficult to reach with a 24-MHz lowpass filter having a pole Q of 3, if it can be reached at all with a 3.3 V design.

In this paper, we present an example which shows that the 24-MHz, $Q = 3$ biquad can be built with an SFDR of at least 50 dB by generating its MOSFET-resistor control voltage by a charge pump. First, we discuss the benefits of having a higher control voltage and the optimum signal swing at the nodes of the MOSFET–C network. Then the effects of a high-frequency control voltage ripple are described. A suitable charge pump is presented, and, finally, the new biquad is compared to the one presented in [2].

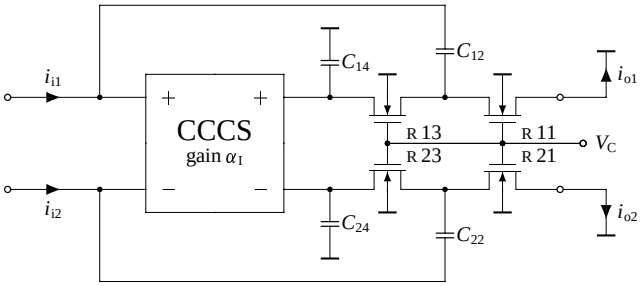

Figure 1: Single-amplifier biquadratic lowpass filter.

2. MOSFET RESISTOR CONTROL VOLTAGE

The control voltage of the MOSFET resistors should be made as large as possible for three reasons: first, the possible voltage swing at the nodes of the MOSFET–C network increases with increasing control voltage; second, the filter's tuning range is also increased, and third, mismatch-induced harmonic distortion is reduced.

If the goal is to build a moderate-linearity filter (i.e. with a harmonic distortion around -50 dB, which is enough for most video-frequency applications), then the maximum voltage at the terminals of the MOSFET resistors should not exceed their pinch-off voltage [3], which is

$$V_p = \frac{V_C - V_{T0}}{m_0} \qquad \text{with} \qquad m_0 = 1 + \frac{\gamma}{2\sqrt{V_{agnd} + \phi_0}} \,. \qquad (1)$$

In (1), V_C is the control voltage of the MOSFET resistor, V_{T0} is its threshold voltage, and m_0 is a factor describing the body effect. The latter is calculated from the body effect parameter γ, the analogue-ground voltage V_{agnd}, and the surface potential of silicon ϕ_0. All voltages are referred to the transistor's body, i.e., to V_{ss} for *n*MOS and to V_{dd} for *p*MOS transistors. Note that the pinch-off voltage does not depend on transistor dimensions, therefore it does not depend on the MOSFET resistance either, provided that short-channel and narrow-channel effects can be neglected.

The maximum possible voltage swing is then approximately the difference between analogue ground and pinch off. For example, if $V_{agnd} = 1.65$ V, $\phi_0 = 0.94$ V, $V_{T0} = 0.85$ V and $\gamma = 0.8\sqrt{\text{V}}$ (i.e. the values of the *n*MOS resistors in our filter), then $V_p = 1.97$ V and 3.01 V for $V_C = 3.3$ V and 4.6 V, respectively. In the latter case, the maximum voltage swing before pinch-off occurs is larger by a factor of 4.25, or by 12.6 dB. As explained in [3], this essentially means that the signal magnitude for which a certain moderate harmonic distortion (e.g. 45 dB) is reached becomes 12.6 dB higher. So does the SFDR, since the filter's noise essentially comes from the CCCS and is hardly affected by the MOSFET resistors' tuning voltage.

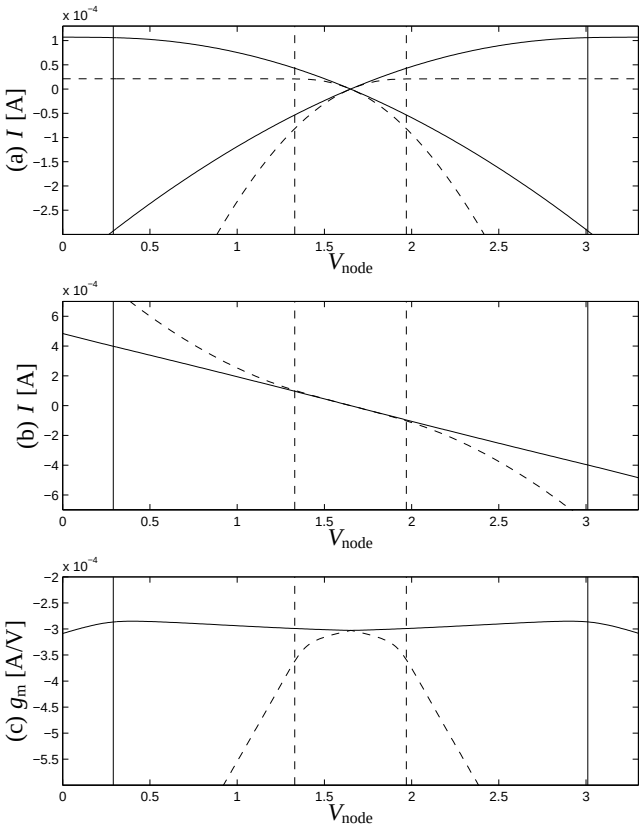

Figure 2: MOSFET resistor pinch-off. Solid: $V_C = 4.6\,\mathrm{V}$. Dashed: $V_C = 3.3\,\mathrm{V}$. (a) DC current through the two balanced paths. (b) Difference of these currents. (c) Slope of the difference (i.e. local transconductance). Vertical lines: pinch-off voltages of the MOSFET resistors.

This theoretical value becomes even larger when second-order effects are taken into account. Fig. 2 shows results of a DC simulation of the circuit in Fig. 1 for $V_C = 4.6\,\mathrm{V}$ (solid) and $V_C = 3.3\,\mathrm{V}$ (dashed). In the former case, both transistors are $12 \times 6\,\mu\mathrm{m}$, in the latter case, they are $29 \times 3\,\mu\mathrm{m}$, such that the same resistance results in the operating point. The voltage at the input of the MOSFET–C network (the output of the CCCS), V_{node}, is swept from 0 V to 3.3 V, i.e. from rail to rail. Fig. 2 (a) shows the currents through both balanced paths and the pinch-off voltages of the MOSFET resistors. Fig. 2 (b) shows the difference of both path currents, i.e. the actual output signal of the filter. The slope of this difference can be seen in Fig. 2 (c). Here it becomes apparent that the possible voltage swing extends beyond the pinch-off voltage for $V_C = 4.6\,\mathrm{V}$, but does not quite reach it for $V_C = 3.3\,\mathrm{V}$.

3. MOSFET–C NETWORK NODE-VOLTAGE SWING

According to Fig. 2 (c), the MOSFET–C network with $V_C = 4.6\,\mathrm{V}$ could actually be driven from rail to rail. Although it is possible to build a CCCS whose output can get arbitrarily close to the rails, this does not necessarily improve the dynamic range and the SFDR of the filter, as we will now demonstrate.

The half circuit of the CCCS used in the filter is shown in Fig. 3. The cascode transistors of the current mirrors and current

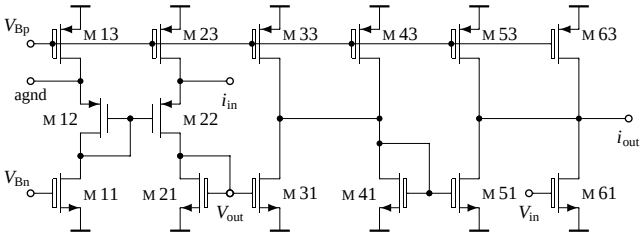

Figure 3: Half-circuit of the CCCS (from [2]). All transistors with box gates are composed of a main transistor and a cascode transistor.

sources in the CCCS are biased with analogue ground (c.f. Fig. 3). Thus the available voltage swing is approximately $\pm 0.85\,\mathrm{V}$, which is the threshold voltage of the *p*MOS transistors. This also means that the voltage margin available to accommodate the saturation voltage V_{dsat} of both transistors in, e.g., the super transistor M 63 is $V_{\mathrm{dd}}/2 - V_{\mathrm{T0}} = 0.8\,\mathrm{V}$ for $V_{\mathrm{dd}} = 3.3\,\mathrm{V}$ and $V_{\mathrm{T0}} = 0.85\,\mathrm{V}$.

Increasing the voltage swing means moving the bias voltage of the cascode transistors closer to the rails by a voltage ΔV. Then the new voltage margin becomes $V_{\mathrm{m}} = V_{\mathrm{dd}}/2 - V_{\mathrm{T0}} - \Delta V$. If the distribution of the voltage margin between the main transistor and the cascode transistor remains the same (i.e. 70 % for the main transistors, 30 % for the cascode transistors), the main transistor's V_{dsat} decreases by a factor of

$$k = \frac{V_{\mathrm{dd}}/2 - V_{\mathrm{T0}}}{V_{\mathrm{dd}}/2 - V_{\mathrm{T0}} - \Delta V}\,. \tag{2}$$

Basically, this can be accomplished by making both transistors wider by a factor of k^2. However, the CCCS must not become slower. Its speed depends on the main transistor's $g_{\mathrm{m}}/C_{\mathrm{gs}} = c \cdot V_{\mathrm{dsat}}/L^2$, where c is a design-independent quantity. To maintain the same speed without changing V_{dsat} again, it is necessary to scale the main transistor's length by $1/\sqrt{k}$ and its drain current I_{D} by $\sqrt{k}$. It then follows from $g_{\mathrm{m}} = 2\,I_{\mathrm{D}}/V_{\mathrm{dsat}}$ that the main transistor's g_{m} becomes $k^{3/2}$ times larger. Finally, the RMS of the noise current is proportional to $\sqrt{g_{\mathrm{m}}}$ and increases by a factor of $k^{3/4}$.

This can now be compared with the increase of the voltage swing,

$$k' = \frac{\Delta V + V_{\mathrm{T0}}}{V_{\mathrm{T0}}}\,. \tag{3}$$

The SNR is thus scaled by $k'/k^{3/4}$. Solving this for the optimum gives an astonishingly simple result:

$$\frac{\mathrm{d}}{\mathrm{d}\,\Delta V}\frac{k'}{k^{3/4}} = 0 \quad\Longrightarrow\quad \Delta V = \frac{2}{7}V_{\mathrm{dd}} - V_{\mathrm{T0}}\,. \tag{4}$$

In our example, $\Delta V = 0.09\,\mathrm{V}$, which is not quite the V_{agnd} used in our CCCS. However, calculating the actual values shows that only 0.1 dB of SNR is lost by connecting the cascode transistors' gates to analogue ground, which by no means justifies using a bias voltage generator.

4. EFFECTS OF A CONTROL-VOLTAGE RIPPLE

The main problem with using a charge pump to generate a control voltage of 4.6 V is that clock feed-through occurs. There are two paths through which the clock has an influence on the filter output current: one is via a ripple on the control voltage, and the other

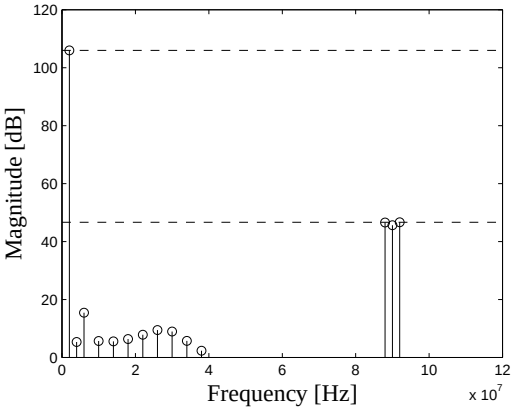

Figure 4: Output current spectrum (0 dB denote 0.5 nA).

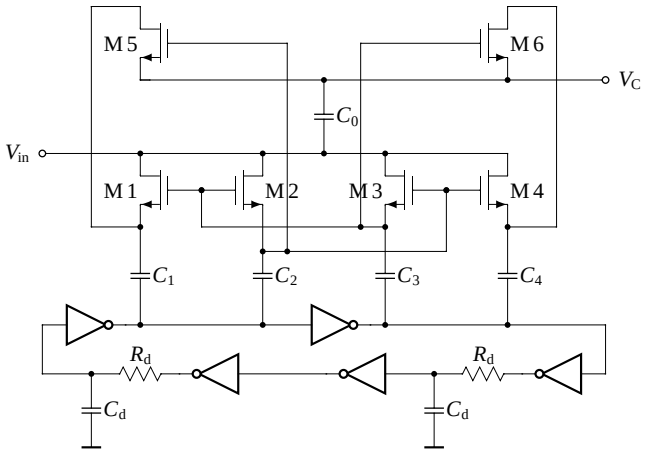

Figure 5: Self-oscillating two-stage charge pump. (The inverters are connected between V_{in} and the chip's V_{ss}.)

is through electro-magnetic coupling and through substrate noise. (This cannot be simulated. See Sec. 8.)

The control voltage ripple is fed through to the output by two very different mechanisms. First, it leaks in through the gate capacitance of the MOSFET resistor. To keep this effect small, the clock frequency f_{clk} must be in the stop-band of the filter. For our 24-MHz lowpass biquad, we chose $f_{clk} \approx 90\,\text{MHz}$. Simulations show that a voltage ripple of 5 mV (c.f. Sec. 5) causes an output current ripple of 10 nA, independent of the signal. Compared to the maximum output current for 50 dB harmonic distortion, 30 μA, this is a ripple of −70 dB, which is negligible. More important than the linear clock feed-through is that the voltage ripple *modulates* the signal. Fig. 4 shows the simulated spectrum at the filter output for a 2-MHz, 10 μA (at the output) signal and a 5-mV, 90-MHz control voltage ripple. It can be seen that mixing products appear at 88 MHz and at 92 MHz. Their magnitude is proportional to the input signal magnitude. Simulations showed that both peaks lie 58 dB below the signal, giving a total distortion of −55 dB, which scarcely affects the 50-dB SFDR of the filter.

All *n*MOSTs	$10 \times 0.6\,\mu\text{m}$
All *p*MOSTs	$33 \times 0.6\,\mu\text{m}$
R_d	4.8 kΩ
C_d, C_2, C_3	0.5 pF
C_1, C_4	1 pF
C_0	20.5 pF

Table 1: Transistor dimensions and component values in the charge pump.

5. SELF-OSCILLATING CHARGE PUMP

The charge pump shown in Fig. 5 combines features of the one proposed by Duisters and Dijkmans in [4] with those of a five-inverter ring oscillator. It actually comprises two charge pumps. The main pump, consisting of M 1, M 4, M 5, M 6, C_1, and C_4, fills the reservoir capacitor C_0 with charge, where M 5 and M 6 alternatively conduct the charging current. A second pump driven by the same inverters, consisting of M 2, M 3, C_2, and C_3, sets the gate voltage of M 5 and M 6 to $2\,V_{in}$ while they charge C_0. Thus the output voltage becomes

$$V_C \leq 2\,V_{in} - V_{T5}\,, \tag{5}$$

where M 5's threshold voltage V_{T5} is comparatively large because of the bulk effect (we are using an *n*-well process). In our example, $V_C = 4.6\,\text{V}$ for $V_{in} = 3\,\text{V}$. The charge pump operates properly for $V_{in} = 1.3 \ldots 3.3\,\text{V}$, resulting in $V_C = 1.5 \ldots 5.3\,\text{V}$.

The voltage ripple of this charge pump is smaller than that of a conventional charge pump by a factor of $g_{m5}/g_{ds5} \approx 30 \ldots 100$. As mentioned in [4], the voltage ripple of a single-stage charge pump is

$$V_{ripple} = \frac{1}{2} \cdot \frac{I_{out}}{C_0\ f_{clk}}\,, \tag{6}$$

where I_{out} is the DC current flowing out of the reservoir capacitance C_0 and f_{clk} is the pump's clock frequency. This means that if V_{ripple}, I_{out} and f_{clk} are the same, the two-stage charge pump needs a reservoir capacitor which is $30 \ldots 100$ times smaller than the one in a conventional charge pump. The fact that it still requires 20.5 pF of capacitance shows that one could not actually afford the chip area a conventional charge pump would use.

The oscillator was built such that its oscillation frequency is well beyond the filter's pole frequency, i.e. around 90 MHz. Since the inverters need to deliver small currents only, they can be built with small transistors. Using only inverters would result in an oscillation frequency of almost 1 GHz, thus two passive one-pole lowpass filters, each consisting of one high-resistive poly resistor and one poly-poly capacitor, had to be used to slow the oscillator down to 90 MHz. This has the additional advantage that it reduces the temperature dependence of f_{clk}. A transient simulation using worst-case process parameters and temperatures showed that the oscillation frequency can be expected to be between 70 MHz and 115 MHz, with a typical value of 93 MHz and a charge-pump output voltage ripple of 4 mV. Table 1 shows the transistor dimensions and component values used in the charge pump.

Fig. 6 presents the layout of the charge pump, the filter, and the V–I converter used for measurement purposes. The charge pump increases the filter's chip area by 60 %. Note that the reservoir capacitor C_0 was placed in between the active parts of the charge pump and the filter for shielding purposes. Note also that there are comparatively large substrate contact bars between the pump and the MOSFET–C network. There is a common guard ring (scarcely

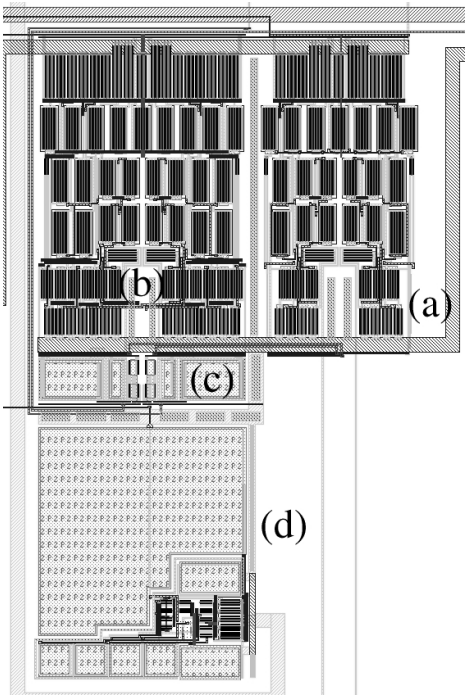

Figure 6: Layout of V–I converter (a), CCCS (b), MOSFET–C network (c), and charge pump (d).

visible in Fig. 6) around the inverters, the pumping capacitors, and the passive filters as well. Finally, the biquad itself was built as described in [2], but using different component values to improve the CCCS's input impedance, its phase lag, its area, and its noise spectrum. The new component values are given in Tab. 2

6. RESULTS

The maximum voltage swing at the MOSFET–C network nodes was slightly below 0.1 V in the filter presented in [2]. This has now been increased to 0.85 V, or by a factor of 18.6 dB. Since mismatch-induced distortion will also be reduced, it is reasonable to expect that the SFDR is larger by at least 18 dB, which is the value given in Tab. 3. The higher SFDR is paid for by an increase of 28 % in power consumption. The chip area is even slightly smaller, since the current mirror transistors in the new CCCS could

	capacitor dimensions	nominal capacitance
C [1–2]2	$46.3 \times 28\,\mu$m	1.13 pF
C [1–2]4	$7.4 \times 28\,\mu$m	0.19 pF

	main transistors	cascode transistors
M [1–6]1	$45 \times 1.8\,\mu$m	$95 \times 0.6\,\mu$m
M 81	$14 \times 0.6\,\mu$m	—
M 91	$45 \times 1.8\,\mu$m	$95 \times 0.6\,\mu$m
M [1–2]2	$120 \times 0.6\,\mu$m $\times$ 2	—
M 13	$87 \times 1.8\,\mu$m	$140 \times 0.6\,\mu$m
M [2–8]3	$70 \times 1.8\,\mu$m	$140 \times 0.6\,\mu$m
M 93	$87 \times 1.8\,\mu$m	$140 \times 0.6\,\mu$m
R [1–2][1–2]	$12 \times 6\,\mu$m	—

Table 2: Transistor and capacitor dimensions in the biquad.

	without pump	with pump	
Pole Frequency	24 MHz	24 MHz	
Pole Q	3	3	
Power consumption	12.4 mW	15.9 mW	+28 %
Chip area	0.12 mm^2	0.11 mm^2	−8 %
SFDR	32 dB	50 dB	+18 dB

Table 3: Comparison of the MOSFET–C biquad (without pump) in [2] and the charge-pump-controlled biquad (with pump) presented here.

be made shorter and the layout is now more compact. If the optimized CCCS had already been used in [2], adding the charge pump would have increased the chip area by 60 %. Finally, note that only one charge pump would be necessary to tune the cut-off frequency of a cascade of several biquads.

7. CONCLUSION

We have demonstrated in this paper that a charge pump can indeed be used to generate the control voltage of MOSFET–C single-amplifier biquads, resulting in filters with an improved spurious-free dynamic range of 50 dB. The effects of the higher control voltage and of its ripple have been discussed in detail, and it has also been shown mathematically that the filter with the best dynamic range is not the one that maximises the voltage swing at the nodes of the MOSFET–C network, but one in which the amplifier (here a CCCS) limits the possible voltage swing to about half the distance between analogue ground and the rails.

8. NOTE ON MEASUREMENTS

Problems with the fabrication process made it necessary that the foundry refabricate the circuit. The delay made it impossible to provide measurement results in this paper. However, experience with a first chip using similar techniques with the same process [2, 3] lets us expect that the simulated values are reliable. It can be assumed that, by the time of display, all measurements will have been completed. A copy of the poster displayed at the ISCAS 2000 can be obtained from the contact author (please request it by e-mail from h.p.schmid@ieee.org).

9. REFERENCES

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