A TUNABLE, VIDEO-FREQUENCY, LOW-POWER, SINGLE-AMPLIFIER BIQUADRATIC FILTER IN CMOS

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ABSTRACT

In this paper, a tunable single-amplifier biquadratic lowpass filter is presented. It consists of one balanced low-gain current amplifier and a second-order MOSFET–C feedback network. The filter was integrated in a double-poly 0.6 µm CMOS process and operates from a 3.3 V power supply. The pole frequency is tunable from 15.2 to 17.2 MHz, the pole Q is 3, the spurious-free dynamic range is at least 60 dB, and the filter consumes only 2.4 mW per pole. Furthermore, the active area used per pole is only 0.06 mm^2. The filter is well suited for low-power video-frequency applications, and demonstrates that the MOSFET–C filter technique can be applied successfully to filters other than those based on integrator-connected topologies.

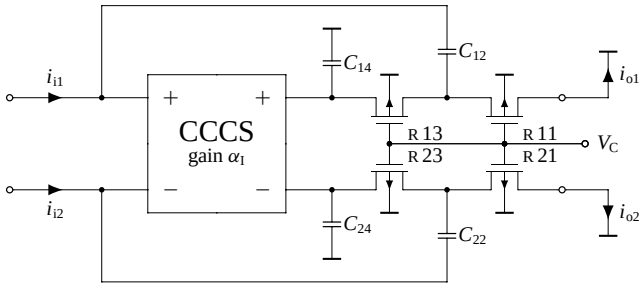

Figure 1: Balanced current signal MOSFET–C Sallen-Key lowpass filter. The bulks of the transistors are connected to V_{dd}.

1. INTRODUCTION

When designing a video-frequency filter for minimum power consumption, it seems reasonable to use as few active components as possible. Good candidates for low-power filters are therefore single-amplifier active RC filters, which produce two or more poles with an RC network in the feedback path of an amplifier. Using a single-amplifier biquadratic lowpass filter (lowpass SAB) as an illustrative example, we demonstrate how such filters can be implemented in CMOS, and also give qualitative design rules for minimizing the power consumption of such filters.

The pole frequency f_p of most active RC filters depends on *absolute* component values, which can vary by up to 20 % in typical CMOS processes, whereas a precision of at least 1 % is normally required. f_p must therefore be tuned. Two ways to achieve this are widely used for implementing integrator-based filters: in so-called g_m–C filters, the integrators are realized by using a tunable transconductance amplifier and a capacitor; in so-called MOSFET–C filters, the resistors are replaced by MOSFETs operating in the triode region, which then have a tunable resistance.

The second solution introduces more harmonic distortion than the first, but since the distortion is mainly of second order, it can be almost completely cancelled out by using a balanced design for the MOSFET–C integrators [1, 2]. The mathematical analysis of such circuits rapidly becomes intractable if applied to second- or higher-order MOSFET–C networks, but there is no theoretical reason why the MOSFET–C principle should not work in these cases as well [3].

In this paper, we present a 17 MHz lowpass SAB with a pole quality factor $q_p = 3$. We chose the Sallen-Key topology[1] for several reasons: first, it is very versatile, since it can be used to build lowpass filters as well as high-pass, band-pass, band-reject and all-pass filters. This is not the case for other classes of SABs [4, 5]. Second, its q_p depends only on ratios of passive components and on the gain of the amplifier, all of which are realizable with reasonable accuracy on a chip. Last, but not least, a high q_p can be realized even with low amplifier gains, if one is prepared to pay for this with higher sensitivity of q_p to variations of the passive component ratios and the amplifier gain.

To optimize these filters for minimum power consumption, an amplifier must be chosen which is just fast enough to realize a filter with a given pole frequency f_p, pole quality factor q_p, and stop-band attenuation A_{stop}. In discrete-component implementations, the low-gain amplifier needed in Sallen-Key filters is normally provided by a high-gain voltage amplifier (opamp) with negative feedback. This stabilizes the gain and reduces harmonic distortion and output resistance by a factor proportional to the feedback loop gain. However, a lowpass filter can still work properly if its f_p is so close to the opamp's unity-gain frequency that the open-loop gain is only about five and the stabilization mentioned above is no longer very effective. Therefore, if power consumption is an important issue, low-gain amplifiers without feedback become attractive: the resulting filter will consume less power, but will also be less linear.

Very fast low-gain open-loop amplifiers can be obtained by combining a low-impedance input stage with a gain stage consisting of current mirrors. For this reason, we used a current amplifier to build a current-signal (or current-mode) filter. Figure 1 shows the circuit diagram of the lowpass filter we have implemented. The balanced current-controlled current source (CCCS, or current amplifier) will be discussed in detail in Section 2, and the the design of the passive network will be explained in Section 3. We used the double-poly double-metal 0.6 µm CMOS process by Austria

[1] We use the terminology "Sallen-Key filter" to designate a non-inverting voltage- or current-based amplifier circuit with an RC bandpass filter in the feedback loop.

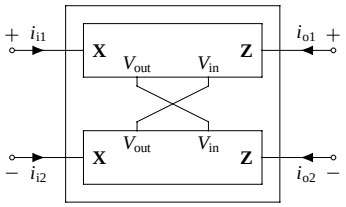

Figure 2: Balanced current amplifier (CCCS).

Mikro Systeme International[2] (AMS CUE process) to implement a cascadable single-amplifier biquadratic filter. Simulation results are presented in Section 4. Compared to other continuous-time filters in the recent literature (e.g. [6–8] (CMOS) and [9] (low-power BiCMOS)), our filter operates at a much higher frequency, is smaller, consumes less power, has comparable distortion and noise performance, but has higher q_p-variations, a narrower tuning range, and needs an additional amplifier as a buffer for off-chip input signals.

2. DIFFERENTIAL-INPUT BALANCED-OUTPUT CCCS

The balanced current amplifier (or CCCS) is based on the same concept as the one published in [3]. It consist of two identical half-circuits, as shown in Fig. 2. This is advantageous, since the harmonic distortion of the filter depends, among other things, on the symmetry of the two signal paths [1, 2]. The ideal current amplifier is described by the equations

$$i_{o1} = \alpha_I (i_{i1} - i_{i2}) \,,$$
$$i_{o2} = \alpha_I (i_{i2} - i_{i1}) \,.$$

The two half-circuits exchange signals by means of two controlling voltages, which will be explained presently.

Fig. 3 shows the amplifier half-circuit. A special symbol has been used for the cascode transistors (see Fig. 4). M [1–6]3[3] and M 11 are constant current sources, while M [2–6]1 form current mirrors. M 22 is the input transistor. It provides, at its source, a current input with input resistance $R_{in} \approx 1/g_{m22}$. M 12 is a voltage level shifter which sets the operating point voltage of node X to analog ground. Any current flowing into X is mirrored from M 21 to M 31 and from M 41 to M 51 and flows out of Z; it is also mirrored from M 21 to M 61 of the other half-circuit, where it flows into Z. Thus the two input currents i_{i1} and i_{i2} are subtracted, and if all current mirrors have unity gain, the resulting gain is $\alpha_I = -2$. In our filter, a gain of $\alpha_I = -2.6$ is required (c.f. [10] or [11, Chap. 75] for design equations), which can easily be achieved by making all output transistors M [5–6][1,3] wider by a factor of 1.3.

Any "super transistor" configuration can be used in Fig. 3, but simple cascodes (Fig. 4) provide sufficient voltage swing, since the voltage swing over the MOSFET resistors critically determines the harmonic distortion of the filter. The higher output resistance of regulated cascode transistors is not needed either, since the output is already capacitive in the frequency region of interest.

As will be shown in Section 4, the signal current at which harmonic distortion becomes larger than 0.1% (−60 dB) is low compared to the bias current. Therefore it was necessary to make the current mirror transistors comparatively long to reduce current offsets caused by mismatch. The cascode transistors are of minimum length, since matching is not an issue there. Because the required voltage swing is only several 100 mV, biasing can be simplified considerably by using analog ground as the bias voltage of the cascode transistors, as indicated in Fig. 4.

[2] `http://asic.vertical-global.com/`

[3] The notation M [1–6]3 denotes "all M i3, where $i = 1 \ldots 6$"

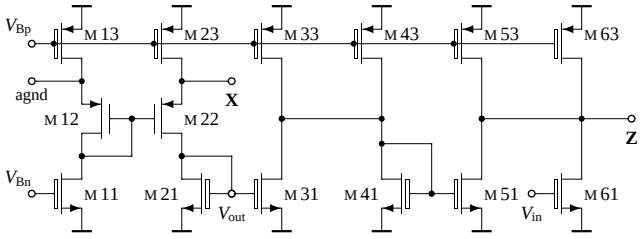

Figure 3: Current amplifier half-circuit.

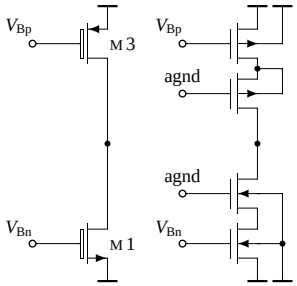

Figure 4: Cascode transistors.

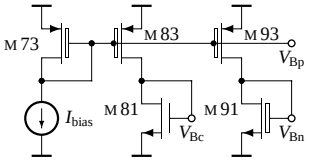

Figure 5: Bias network.

It is apparent that the cascode transistor of M 11 cannot be biased by analog ground, since the gate voltage of M 12 is too low. Fig. 5 shows the bias circuitry which generates the bias voltages for both half-circuits. The voltage generated by the single transistor M 81 biases the cascode transistors of M 11 and M 91. The current source I_{bias} is located off-chip for test reasons.

All nodes of this amplifier are of similarly low impedance and have similar node capacitances. Thus the current transfer function does not have a dominant pole, and cannot be described by a simple mathematical model, although good results can be achieved by using an ad-hoc linear-phase model [10].

3. THE MOSFET–C FEEDBACK NETWORK

The feedback network in Fig. 1 consists of poly–poly capacitors and MOSFET resistors. In the AMS CUE process, γ_{nMOS} (body effect parameter) is much larger than γ_{pMOS}. This means that the channel of an nMOS resistor will be inverted less strongly than the channel of a pMOS resistor at the same operating point voltages.

Figure 6 shows measurements and BSIM 3v3 simulations of nMOS and pMOS test transistors of size $20 \times 3\,\mu$m at five different places on the same test wafer. Their operating point was set as it would be in the filter: the gate controlled by a voltage V_C near the negative rail, the bulk connected to the positive rail, the drain connected to analog ground (mid-rail), and the source varied around analog ground to measure the resistance in the operating point. Note that $\Delta V_C = V_{dd} - V_C$ for nMOS and $V_C - V_{ss}$ for pMOS transistors. The body effect can be seen clearly in Fig. 6: not only do the nMOS curves show much larger variations and curvatures than the pMOS curves, the BSIM 3v3 model is quite inaccurate as well for nMOS resistors. Similar comparisons made for test transistors of different size showed similar results. Therefore, although being slower, pMOS resistors must be used for low-voltage MOSFET–C filters, since they have both lower variations and lower distortion.

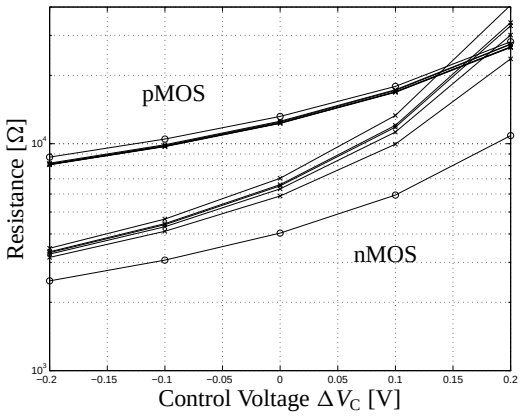

Figure 6: Resistance of $20 \times 3\,\mu$m MOSFET resistors. ($\times$) five measurements at different places on the same wafer. ($\circ$) BSIM 3v3 simulations.

Neither the feedback components nor the amplifier can be described accurately by simple models at 17 MHz. The best way to design such a filter is therefore iteratively: first design the amplifier, then the MOSFET–C network, and then improve the filter, improve the network, and so on. It was shown in [10] that the maximum pole frequency achievable with a certain amplifier is

$$2\pi f_{\mathrm{p\,max}} \approx \frac{1}{10\, C_{\mathrm{out}} R_{\mathrm{in}} A_{\mathrm{stop}}}\,, \qquad (1)$$

where C_{out} and R_{in} are the amplifier's output capacitance and input resistance, and A_{stop} is the stopband attenuation of the filter. This formula is accurate if the passive component spread is kept low, and if the amplifier's phase lag at the pole frequency is not higher than a few dozen degrees. Keeping (1) in mind, we observed the following qualitative design rules while designing our filter:

(i) Reducing R_{in} increases $f_{\mathrm{p\,max}}$. This can be achieved in three ways: (a) by making M [1–2]2 shorter, which increases the voltage offset between analog ground and X. (b) by making M [1–2]2 wider, which increases the amplifier's phase lag. (c) by increasing the amplifier's bias current, which increases C_{out} (because all current mirrors must then be made wider to maintain the same input voltage swing) and therefore counters the increase of $f_{\mathrm{p\,max}}$.

(ii) Reducing C_{out} also increases $f_{\mathrm{p\,max}}$. This means making the cascode transistors of the current mirrors narrower, which reduces the drain-source voltage of the main transistors. Thus the bias current must be reduced to keep the main transistors in saturation, which again increases the amplifier's phase lag.

(iii) The amplifier's phase lag must be low enough. Again, there are two ways to decrease the phase lag: (a) The bias current is increased, with the side effects described in (i)(c). (b) The current mirror transistors are made shorter. This increases the output current offset and therefore causes an imbalance, increasing the harmonic distortion of the whole filter.

(iv) The MOSFET resistors have parasitic capacitances in parallel to the poly–poly capacitors. Therefore reducing their size increases $f_{\mathrm{p\,max}}$. Since our MOSFET resistors are wide rather than long, reducing their size means increasing their resistance. This makes it necessary to decrease the feedback capacitances and also C_{out}. On the other hand, it also allows to increase R_{in}.

The optimum design depends critically on which non-idealities are important, and which ones are not. In our case, input voltage offset is not critical, so we used minimum-length input transistors in our design. Harmonic distortion, however, is critical. To be on the safe side, we made the current mirror transistors comparatively wide (3 μm). We designed our filter to have a comparatively small stopband attenuation of 30 dB, which is sufficient if this filter section is cascaded to form higher-order filters (e.g. 60 dB for a fourth-order filter).

The transistor sizes are shown in Table 2. The whole filter is operated with a bias current of 80 μA from a ± 1.65 V supply, giving it a total power dissipation of only 4.8 mW.

	nMOS	pMOS	
V_{T0}	0.85	-0.92	[V]
$\mu \cdot C_{\mathrm{ox}}$	120	40	[μA/V^2]
γ	0.8	0.5	[$\sqrt{\mathrm{V}}$]

Table 1: Typical threshold voltages, transconductance parameters and body factors of the 0.6 μm CMOS process by Austria Mikro Systeme (AMS CUE).

#	capacitor dimensions	capacitance
C [1–2]2	$13.6 \times 13.6\,\mu\mathrm{m} \times 10$	1.0 pF
C [1–2]4	$13.6 \times 13.6\,\mu\mathrm{m}$	0.1 pF

#	main transistors	cascode transistors
M [1–4]1	$45 \times 3\,\mu$m	$80 \times 0.6\,\mu$m
M [5–6]1	$57.3 \times 3\,\mu$m	$104 \times 0.6\,\mu$m
M 81	$37.3 \times 3\,\mu$m	—
M 91	$45 \times 3\,\mu$m	$80 \times 0.6\,\mu$m
M [1–2]2	$120 \times 0.6\,\mu\mathrm{m} \times 2$	—
M [1–4]3	$120 \times 3\,\mu$m	$200 \times 0.6\,\mu$m
M [5–6]3	$200 \times 3\,\mu$m	$260 \times 0.6\,\mu$m
M [7–9]3	$120 \times 3\,\mu$m	$200 \times 0.6\,\mu$m
R [1–2]1	$22 \times 2.4\,\mu\mathrm{m} \times 2$	—
R [1–2]2	$22 \times 1.9\,\mu\mathrm{m} \times 2$	—

Table 2: Transistor and Capacitor Dimensions.

4. SIMULATION RESULTS

The circuits described in the previous section were fabricated in the AMS CUE CMOS process (see Table 2).[4] Fig. 7 shows part of the layout, two identical biquads on one chip. The block denoted "amp" is a voltage-to-current converter, which is necessary because the comparatively high input resistance of the SAB forms a pole at approximately 20 MHz together with the pad capacitance.

Figure 8 shows the simulated frequency response of the biquad for $V_{\mathrm{C}} = V_{\mathrm{ss}}$, showing the desired stopband attenuation of 30 dB.

Figure 9 shows how the peak in the frequency response moves towards lower frequencies if the gate voltage of the MOSFET resistors is tuned from $V_{\mathrm{C}} = V_{\mathrm{ss}}$ to $V_{\mathrm{C}} = V_{\mathrm{ss}} + 0.1$ V. The pole frequency decreases from 17.2 to 15.2 MHz, while the pole quality factor increases from 3.0 to 3.78. If this dependency of q_{p} on V_{C} is too strong for a particular application, then either the amplifier's input resistance must be reduced, or q_{p} must be tuned, both of which costs power.

[4] Unfortunately, measurements could not yet be made because of delays in the fabrication of the measurement circuits. Results should be available very shortly. We are confident that the measurement results will be similar to the simulations, since the models correspond well to the measured test transistors (c.f. Fig. 6).

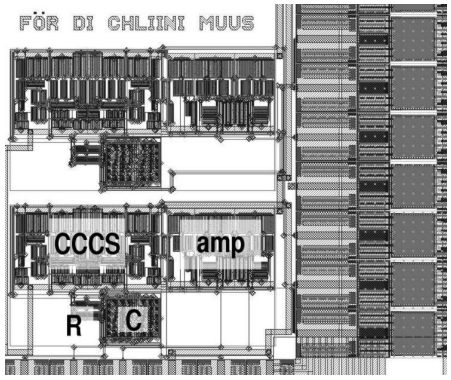

Figure 7: Layout extract showing two biquads and some pads.

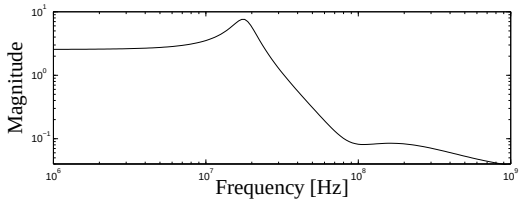

Figure 8: Frequency response for $V_C = V_{ss}$

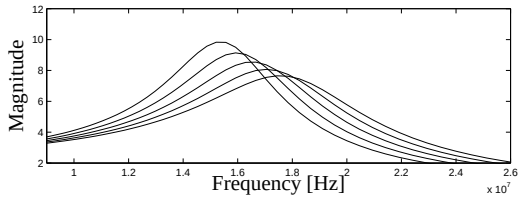

Figure 9: Frequency response for $V_C = V_{ss} + 0\,\mathrm{V} \ldots 0.1\,\mathrm{V}$.

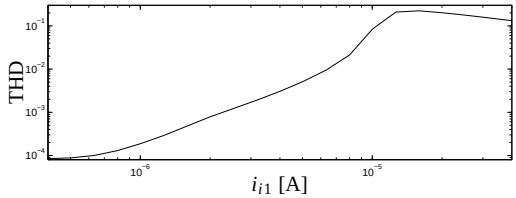

Figure 10: Total harmonic distortion for a 3.2 MHz balanced-input signal (five harmonics in the filter's pass-band).

The THD of the balanced output signal as a function of the input current magnitude is shown in Fig. 10. It is mainly caused by the non-linearity of the MOSFET resistors. Up to a magnitude of $i_{i1} = 2\,\mu\mathrm{A}$, the THD remains below 0.1 % (−60 dB). Noise simulations show that THD is dominant at this input signal level, thus the spurious-free dynamic range (SFDR) of the filter section is at least 60 dB. At a THD of 1 %, the SNR becomes > 65 dB.

5. DISCUSSION AND CONCLUSION

The main limitation of applying the MOSFET–C technique to low-voltage filters are the non-linearity introduced by the MOSFET resistors and their comparatively high resistance. Both can be reduced by increasing the controlling voltage, either by moving the analog ground closer to the positive rail, or by using nMOS resistors controlled by a voltage above the positive rail. The first solution has the disadvantage that biasing becomes more difficult and that the pMOS current sources will become larger and therefore slower. The second solution requires a charge pump with a very low ripple (c.f. [12]). Further investigations will tell whether the resulting clock feed-through from the charge pump to the filter output is weak enough for practical applications.

We have shown in this paper how to build a tunable video-frequency lowpass filter section with tunable pole frequency ($16 \pm 1\,\mathrm{MHz}$) and a pole-Q of $3.4 \pm 10\,\%$. It could be used, for example, as the highest-Q biquadratic section of a ninth-order Butterworth filter. We have also discussed in detail the numerous trade-offs which must be kept in mind when designing such a filter. All in all, this demonstrates that the MOSFET–C filter technique can be applied successfully to single-amplifier biquadratic filters.

6. ACKNOWLEDGEMENTS

We would like to thank Ehrenfried Seebacher from AMS for providing a wafer containing test transistors, Władysław Grabiński for measuring the transistors and extracting transistor parameters, and Felix Frey for developing the off-chip measurement circuits necessary to measure our filters.

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[Note: A copy of the poster to be displayed at the ISCAS '99 can be obtained from the contact author (please request it by e-mail from the contact author, h.p.schmid@ieee.org). It can be assumed that, by the time of display, all measurements will have been completed.]